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A 5.4μm^2 Sheath-Plate-Capacitor DRAM Cell with Self-Aligned Storage-Node Insulation

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A novel trench-capacitor DRAM cell structure named a Sheath-Plate-Capacitor (SPC) cell with self-aligned storage-node insulation for 16M bits has been developed by using a 0.6um process technology. The SPC cell has achieved a small cell area of 5.4um^2, very low trench to trench leakage current characteristics and high alpha-particle immunity (critical charge=35fC) by using a sheath plate structure and three new self-alignment technologies: (1) sidewall contact, (2) storage node insulation, and (3) a pad for bit-line contact. The device was evaluated using an experimental 4K-bit array.

1. INTRODUCTION

How to enlarge storage charge is one of the most important problems in the fabrication of highly integrated DRAMs such as 4M, 16M or beyond. To achieve this objective, three dimensional cell structures, such as the trench-capacitor type cell[1,2] and the stacked capacitor type cell[3], have been proposed. Although the trench type cell has good potential to attain this enlargement, it must solve two basic issues, (1) trench to trench leakage current and (2) alpha-particle immunity. This is because its storage-node, which exists in a Si substrate, is directly influenced by the electrical phenomena in the Si substrate.

In this paper, a new trench-capacitor DRAM cell named Sheath-Plate-Capacitor (SPC) cell will be described. The SPC cell is characterized by an inner storage node and a highly self-aligned cell structure. The inner storage node, which is covered by a sheath electrode and an insulating layer, is expected to achieve both low trench-to-trench leakage current characteristics and a good immunity to alpha-particle injection. The highly self-aligned cell structure, which is fabricated by using three self-alignment techniques, provides a small cell area of 5.4um^2 (1.5 x 3.6) for 16M-bit DRAM.

2. CELL STRUCTURE AND FABRICATION PROCESS

A scanning electron micrograph of a cross section of an SPC cell is shown in Fig.1. Because a storage-node electrode is surrounded by a sheath-plate and an SiO_2 sheath, this inner node is electrically isolated from the Si substrate. Therefore, a punchthrough phenomenon between adjacent trench capacitors can be theoretically eliminated. The word-line is isolated from the storage-node by the SiO_2 layer which is fabricated by using a self-aligned oxidation technique. This storage electrode is connected with a drain diffused layer of a transfer MOS transistor through a self-aligned sidewall contact. This contact structure

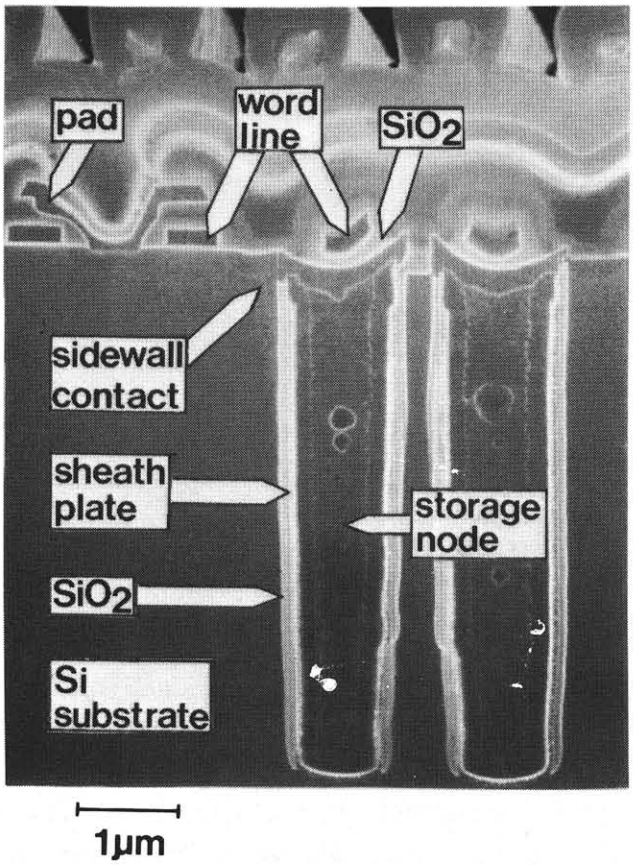

Fig.1 Scanning electron micrograph of a cross section of SPC.

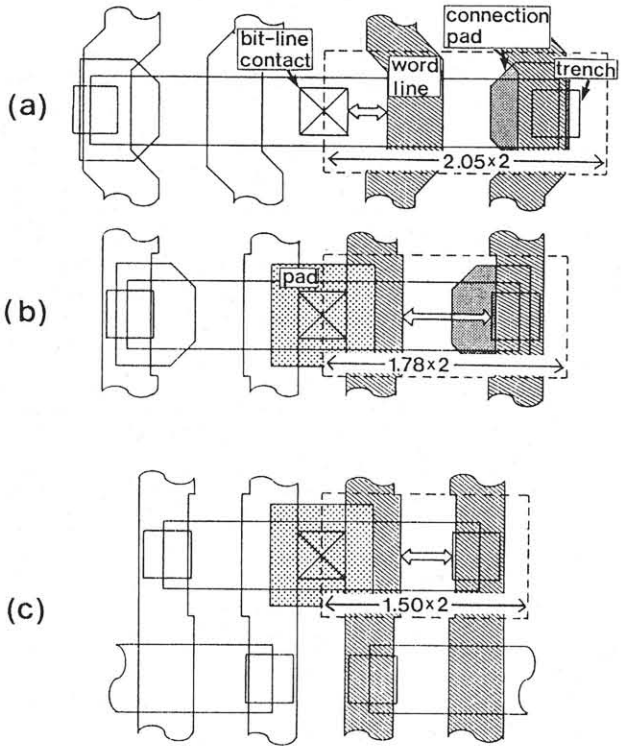

Fig.2 Effects on self-alignment technologies in SPC layout.
(a) conventional structure,
(b) pad structure,
(c) pad and sidewall contact structures.

enables decrease in trench to transistor distance. A pad structure also decreases the word-line pitch by eliminating the contact-hole to word-line space.

Because a sheath plate is electrically connected with the Si substrate via the bottom of the groove, plate voltage is controlled by the substrate voltage. Therefore, 0V or a small negative substrate voltage is desirable for memory operation from the viewpoint of a time-dependent dielectrically-breakdown phenomenon in capacitor insulators.

Effects on self-alignment structures are shown in Fig.2. This figure shows three types of layouts for the SPC cell. A conventional layout method is used in Fig.2 (a). In this type of layout, a large margin is needed for preventing both (1) a short circuit between a bit-line contact and a word-line, and (2) electrical disturbance in a transfer MOS transistor, which is caused by the approach of an n^+ diffused layer under a connection pad to this transistor. The former problem is solved by introducing the pad structure shown in Fig.2 (b). This eliminates the space between the contact and word-line; the word-line pitch can be reduced by 0.27um. For the latter problem, a self-aligned sidewall contact structure is a good solution for minimizing the trench to transistor distance. By using this, the connection pad can be eliminated and the word-line pitch can be further reduced by 0.28um (Fig.2 (c)). By using these techniques, the word-line pitch can thus be decreased by 0.55um to obtain a 1.5um word-line pitch.

The fabrication process of the SPC cell

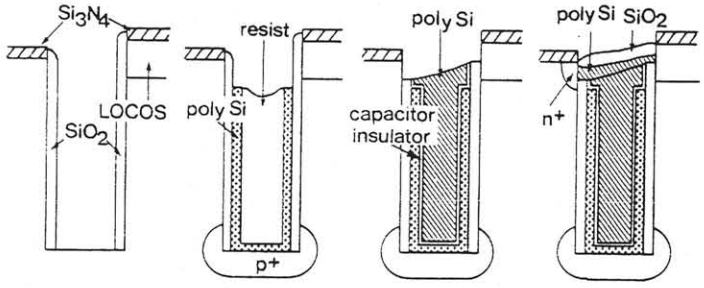

Fig.3 Process flow of the SPC cell.

is shown in Fig.3. After a 5um deep Si groove is formed at a LOCOS edge, an SiO_2 sheath is formed by using reactive ion etching followed by CVD SiO_2 deposition (Fig.3 (a)). Sheath poly-Si is deposited and boron is doped by using a gas phase diffusion technique which uses BN plates as a diffusion source. The poly-Si is etched by using an isotropic dry etching technique, and a sheath plate is formed. A buried resist is used as an etching mask (Fig.3 (b)). After a 12nm SiO_2-equivalent tri-layer (SiO_2-Si_3N_4-SiO_2) insulating film and a poly-Si storage-node are formed, SiO_2 at the location of a side-wall contact is etched off by using an HF solution (Fig.3 (c)). Finally, the surface of the poly-Si storage-node is oxidized followed by CVD poly-Si deposition (Fig.3 (d)). During oxidation, a sidewall contact is formed by a diffusion of phosphorus.

As shown in this figure, only one photolithography process is required for fabrication of the SPC structure by using a fully self-aligned SPC process.

The SPC process has full compatibility with the CMOS process. Therefore, a high-speed and low-power CMOS SPC DRAM can be easily produced.

3. ELECTRICAL CHARACTERISTICS OF SPC CELL

Because of its sheath-plate structure,

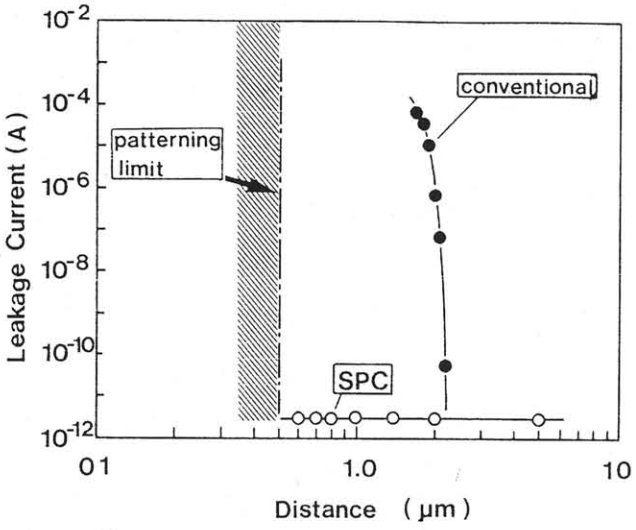

Fig.4 Trench to trench leakage current characteristics.

the trench to trench leakage current in the SPC cell is negligibly small compared with that in the conventional trench capacitor cell[4] as shown in Fig.4. Therefore, a close trench capacitor layout such as 0.5um spacing is actually possible.

A small area of n^+ diffused layer in the SPC cell is advantageous for attaining good memory-retention characteristics. Figure 5 shows temperature dependence of retention

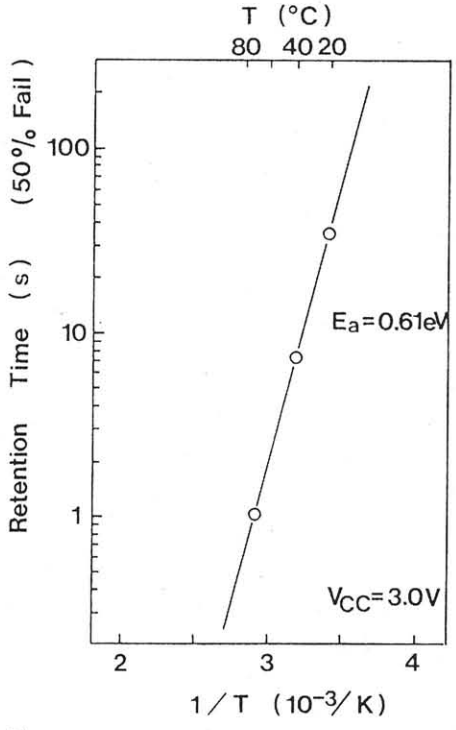

Fig.5 Temperature dependence of retention time.

time. Here, retention time is defined as the time at which 50% of the bits in an experimental 4K bit array fail. A retention time of the SPC cell was evaluated 40 seconds at 20C. Using these results, the activation energy of the retention time is estimated as 0.61eV. This value is very close to half of the Si band gap energy, which shows that the leakage phenomenon in the SPC cell is due to junction leakage current.

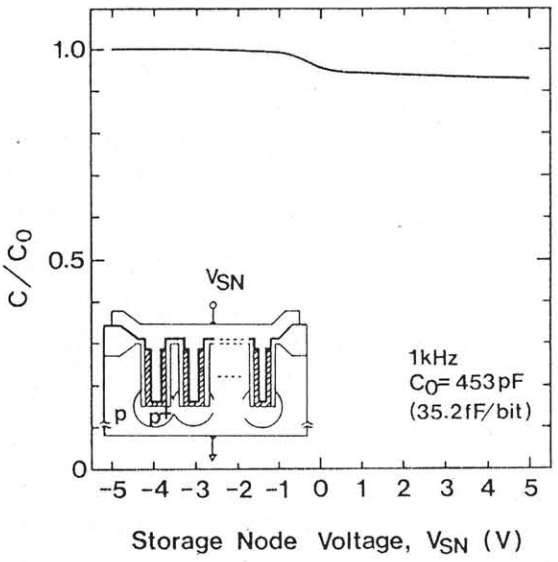

Fig.6 Storage-node voltage dependence of capacitance of sheath plate capacitor.

In the SPC cell, a large capacitance of 35fF/bit (58fC/bit at 3.3V operation) has been achieved. The heavily doped plate structure in the SPC cell provides a small reduction of capacitance as shown in Fig.6.

A critical charge in the SPC cell was measured to be 35fC by using a compulsory irradiation method of alpha-particles. This value shows that the alpha-particle immunity of this cell is satisfactory.

4. CONCLUSION

A novel trench capacitor structure (SPC) for 16M bit DRAM has been developed by using a 0.6um process technology. Having a sheath-plate structure and using three self-alignment technologies, the SPC cell attains a small cell area of 5.4um^2 (1.5 x 3.6), a long retention time of 40 seconds at 20C, and high alpha-particle immunity (critical charge = 35fC).

As a result of our evaluations, we conclude that the SPC cell is a promising device for 16M-bit DRAMs and beyond.

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