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A 5.4μm^2 Stacked Capacitor DRAM Cell with 0.6μm Quadruple-Polysilicon Gate Technology

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A 5.4um^2 stacked capacitor DRAM cell is realized using a quadruple-polysilicon gate structure and 0.6um pattern delineation technology. Memory operation in an experimental 4-Kbit array is successfully observed. A 5nm dielectric composite film and storage node pattern optimization by computer simulation are used to realize increased storage capacitance in this small cell. Charge retention characteristics and alpha particle immunity are favorable, indicating that this cell is a good candidate for application to 16 megabit DRAMs.

INTRODUCTION

As the memory cell size decreases in DRAMs, it has become necessary to replace conventional planar cells with three-dimensional cell structures such as a stacked capacitor cells (STC)[1-2] or trench capacitor cells[3] in order to obtain sufficient storage capacitance(Cs). Among the several candidate cell structures for DRAMs, trench capacitor cells have been considered promising for the 4-megabit level and beyond. This is because it is difficult for the STC cell to obtain sufficient Cs if the trend in cell-size reduction continues. However, one of the advantages of the STC cell is that conventional VLSI technology can be readily applied to the fabrication of STC cell.

In this paper, a quadruple-polysilicon gate STC structure and the use of computer simulation for the optimization of mask patterns for Cs enlargement are introduced. These methods make it possible to realize a 5.4um^2 (1.5x3.6 um^2) STC cell with current 0.6um pattern delineation technology. In addition, acceptable memory performance is observed in an experimental 4-Kbit memory arrays. The present cell is suitable as a candidate for application to 16 megabit DRAMs.

QUADRUPLE-POLYSILICON GATE STC CELL

In this section, the present quadruple-polysilicon gate STC cell is compared with the triple-polysilicon STC cell[2] which has already been used in 1 or 4 megabit DRAMs. The triple- and quadruple-STC cells are shown schematically in cross section in Fig. 1. The triple STC features advantages such as (1) the storage capacitor and pad for bit-line contact can be fabricated in the same polysilicon layer, and (2) memory cell is not significantly higher than the surrounding transistors. Thus, high productivity is one of the characteristics of the triple STC cell. However, the large alignment tolerance needed to prevent the plate and pad from shorting becomes a major obstacle to cell size reduction. In the quadruple STC, on the other hand, since an SiO_2 interlayer exists between the storage capacitor and pad, it is not necessary to take the above mentioned

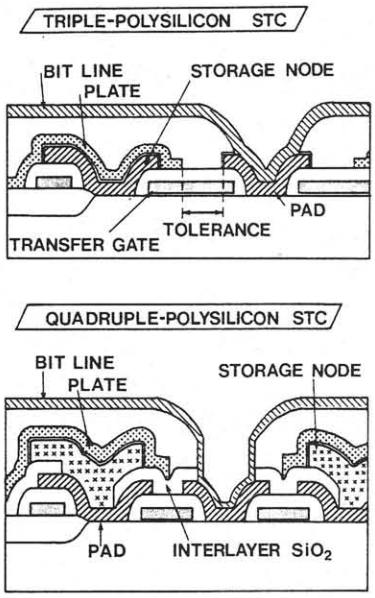

Fig. 1 Comparison of triple- and quadruple STC cell.

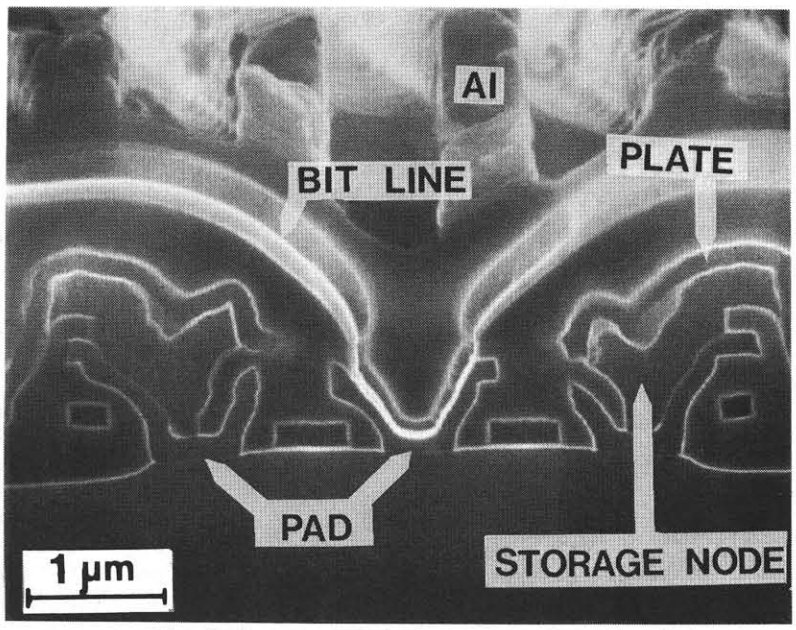

Fig. 2 Cross sectional SEM photograph of fabricated quadruple STC cell.

alignment tolerance into consideration when designing this memory cell. Therefore, the word-line pitch can be reduced remarkably. With this cell structure and 0.6um pattern delineation technology utilizing an i-line aligner, 5.4 um^2 memory cell size can be achieved.

Figure 2 shows the cross sectional SEM photograph of the fabricated quadruple STC. Polysilicon is used in the word-line, pad, storage capacitor and cell plate. The polysilicon pad existing below the storage capacitor is one of the characteristics of the present quadruple STC. As Fig. 2 clearly shows, every layer must be delineated on the underlayer with high steps. Therefore, a triple-layer photolithography and sidewall protecting dry-etch method [4] are used to realize a precise delineation without undercuts.

A twin-tub CMOS structure is used. The gate length and width of the memory cell transistor is 0.9um and 1.0um, respectively. A conventional LDD is used for both the n/p channel transistor and the memory cell transistor. 3.3V Vcc is adopted to improve the reliability of the submicron memory cell transistor.

ENLARGEMENT OF STORAGE CAPACITANCE

The half-Vcc precharge method makes it possible to apply the equivalent of 5nm SiO_2 composite film to the storage capacitor, because the voltage applied to the capacitor dielectric film is reduced to 1.65V.

In order to investigate the reliability of this thin dielectric film, TDDB (Time Dependent Dielectric Breakdown) characteristics are measured (Fig. 3). Film lifetime, defined as the stress time at which 50% cumulative failure takes place, is much longer than that for 9nm film at the half-Vcc(1.65v) voltage.

These results clearly indicate that even 5nm composite film has a favorable reliability as a capacitor dielectric film.

However, even though this 5nm film is used, Cs is calculated to be only 17fF, i.e., 28fC at half-Vcc operation in the 5.4 um^2 STC cell. This charge is found to be smaller than that required for alpha particle immunity.

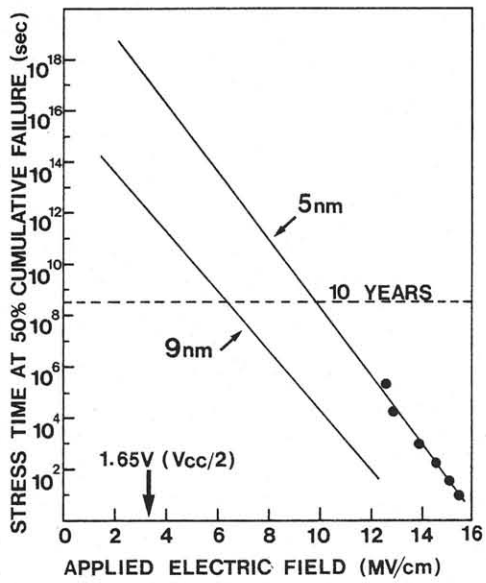

Fig. 3 TDDB characteristics of capacitor dielectric film.

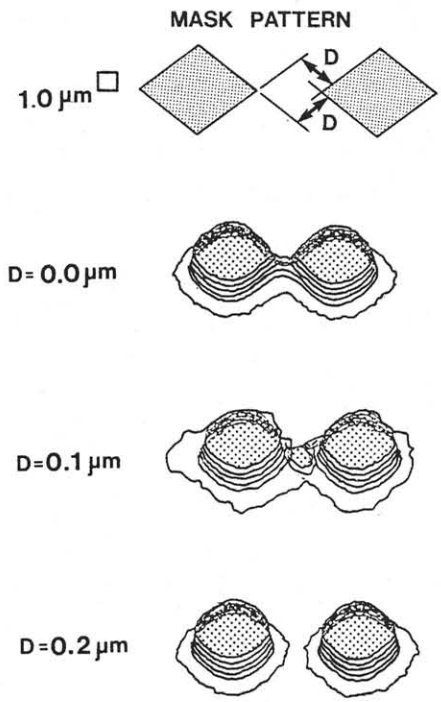

Fig. 4 Computer simulated resist patterns with various spacings between corners.

Thus, the storage node pattern is optimized using computer simulation [5] in order to further Cs enlargement.

A storage node in the STC is designed as a pattern with several corners. The spacing between neighboring corners becomes wider than the designed spacing because of a pattern rounding. This phenomena occurs due to the diffraction effect of projected rays. Therefore, it is possible to make the spacing of the neighboring corners even more narrow than that permitted by the design-rule.

This assumption is verified by the computer simulation. Figure 4 shows the simulated resist patterns with various spacings(D). A TSMR8800 photoresist and an i-line wavelength of 3650A (NA=0.42) are assumed for the simulation. It is found that even 0.2um spacing can be resolved.

Figure 5 compares the calculated stored charge of the optimized pattern with the charge stored in a conventional capacitor. Using the optimized storage node pattern, a charge of 45fC (Cs of 27fF for half-Vcc operation), which is sufficient for alpha particle immunity is expected.

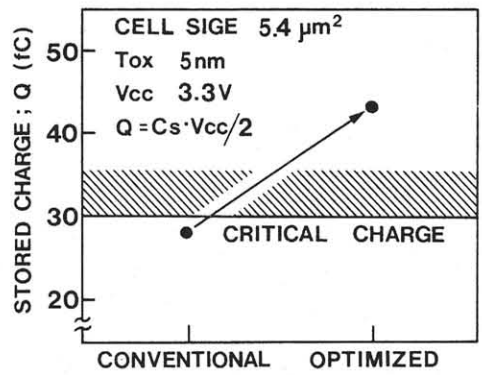

Fig. 5 Calculated stored charges in optimized-pattern cell and conventional cell.

MEMORY OPERATION

Utilizing above mentioned technologies, an experimental 4-Kbit memory array was fabricated and successful memory operation was observed. Average storage capacitance, measured for the 4-Kbit memory, was 28fF. This Cs is in good agreement with the estimated in Fig. 5. Optimization of the storage node pattern is found to be very effective for Cs enlargement.

A precise method for determining S/N revealed that the critical charge for alpha particle immunity was less than 30fC, which is much smaller than the stored charge in the present cell. A small n+ layer in the STC is very useful in reducing collection of alpha-particle-induced charges. Retention time, defined as the time at which 50% of the bits fail, was evaluated to be 40 seconds at room temperature (Fig. 6).

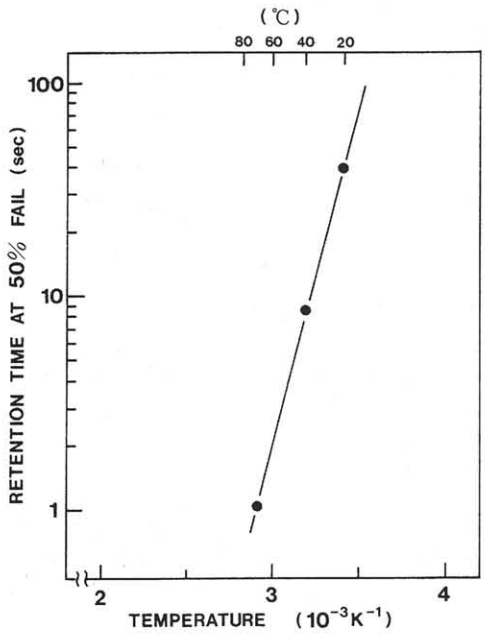

Fig. 6 Temperature dependence of retention time in present STC cell.

CONCLUSION

A stacked capacitor cell with the cell size of 5.4 um^2 was achieved utilizing a quadruple-polysilicon gate structure and 0.6um pattern delineation technology. Optimization of the storage node pattern was found to be very effective for the enlargement of the Cs. The critical charge for alpha particle immunity was measured to be less than 30fC. The charge retention characteristics are also favorable for memory operation.

The present STC cell is thought to have potential as a candidates for forthcoming 16 megabit DRAMs.

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REFERENCE

(1) M. Koyanagi, H. Sunami, N. Hashimoto, and M. Ashikawa, Technical Digest, IEDM, 1978, p. 348.

(2) H. Mochizuki, Y. Kodama, T. Nakano, T. Ema, and T. Yabu, Dig. Tech. Papers, ISSCC, 1987, p. 284.

(3) H. Sunami, T. Kure, N. Hashimoto, K. Itoh, T. Toyabe, and S. Asai, Technical Digest, IEDM, 1982, p. 806.

(4) K. Tsujimoto, S. Tachi, K. Ninomiya, K. Suzuki, S. Okudaira, and S. Nishimatu, Extended Abstract, SSDM, 1986, p. 229.

(5) A. Moniwa, T. Matuzawa, T. Itoh, and H. Sunami, IEEE computer-aided design of integrated circuits and systems, CAD-6, No. 3 1987, p. 431.