

MeV-Boron Implanted Buried Barrier for Soft Error Reduction in Megabit DRAM

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The soft error rate (SER) reduction by an MeV-boron implanted buried barrier is presented in applying a 1Mbit NMOS DRAM. Improvement by a factor of more than X100 was obtained in the bit line mode SER and also by a factor of X50 in the cell mode SER compared with the HiC structure. With the aid of the buried barrier, less than 100 FIT of the SER would be achieved in megabit DRAM with the storage capacitance of 24fF at 5V operation.

1. INTRODUCTION

Alpha-particle induced soft errors have been one of the most important factors in the design of VLSI memories. A lot of experimental and theoretical investigations have been developed to improve soft error rate (SER) together with device structural modifications. The soft errors in the dynamic RAM (DRAM) are classified into two modes i.e., the cell mode and the bit line mode according to the position of alpha-particle hit incidents. HiC (1) and stacked capacitor cells (2) are very effective in reduction of the cell mode SER, however the bit line mode has been remained unimproved because bit lines are not protected against charge collection. The total SER of those memory cells is dominated by the bit line mode, and is inversely proportional to the cycle time. Improvement of the bit line mode SER will become more and more important in future megabit DRAM's. A buried barrier structure, which has high boron concentration region in

the substrate at memory cell areas, is very effective in the SER reduction of both the cell and the bit line modes. The threshold voltage of transistors can be controlled easily in this structure, because the buried barrier is formed far from the surface. The buried barrier structure is favorable as a countermeasure of the soft errors in next generation DRAM's. Wordeman et al. showed that the buried barrier reduces the SER by a factor of X5 in 1um design rule DRAM by simulation (3).

In this paper, we present the SER reduction effects of 1Mbit DRAM with the buried barrier formed by an MeV-boron implantation. Discussions are developed about relations between the SER of 1Mbit DRAM and the charge collection efficiency of alpha-particle induced noise charge measured by using test vehicles.

2. DEVICE STRUCTURE

The MeV-boron implanted buried barrier

was formed in the 1Mbit DRAM with 1.2um design rule, having N-channel planar cells with HiC structure. The MeV-boron implantation was carried out after forming the polysilicon cell plate, which resulted in a shallower barrier underneath the cell plate and a deeper barrier elsewhere, as shown in Fig.1. Consequently the buried barrier does not affect the threshold voltage of transistors, and the change of the bit line capacitance is suppressed in a small increase.

The boron implanted energy and dose examined were 0.7 to 1.8MeV and $1E12$ to $3E13/cm^2$, respectively. Figure 2 shows the typical doping profile under a bit line N^+ , measured by SIMS after completion of fabrication processes. 1MeV-boron implantation with a dose of $1E13/cm^2$ formed a buried barrier peaked at $1.67\mu m$ deep with a peak concentration of around $2E17/cm^3$, two orders of magnitude higher than the substrate doping.

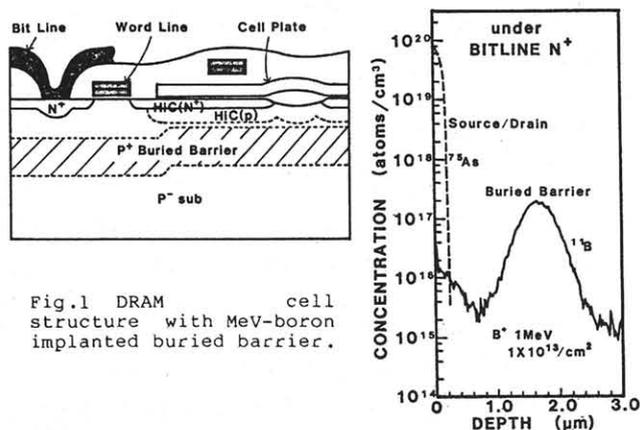


Fig.1 DRAM cell structure with MeV-boron implanted buried barrier.

Fig.2 Doping concentration of buried barrier under bit line N^+ .

The charge collection efficiency of the buried barrier structure was measured with a test vehicle having a $400 \times 500 \mu m^2$ N^+/p junction, and compared with the HiC structure and the p^-/p^+ epi substrate. Figure 3 shows the measured charge collection efficiency as a function of boron implant dose for the buried

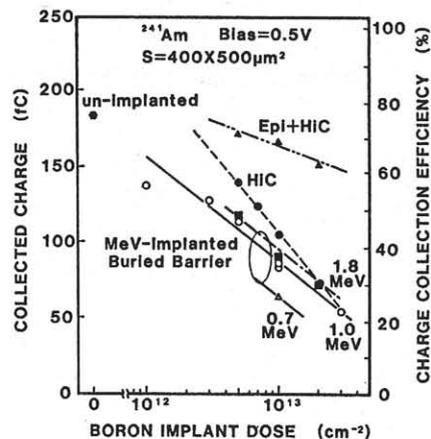


Fig.3 Charge collection efficiency as a function of boron implant dose for buried barrier or HiC(p) formation.

barrier or the HiC(p) structures. The charge collection efficiency decreased with an increase of a boron implant dose, and was 40-50% of that of the unimplanted sample at a dose of $1E13/cm^2$. The buried barrier was more effective in reducing the charge collection efficiency than the HiC structure with the same boron dose. This tendency becomes remarkable in increasing bias voltage of N^+/p junction. Because in the HiC structure the highest boron concentration region near the surface was covered with the HiC(N^+) region, thereby the boron concentration effect as a barrier became lower than that of the buried barrier structure. In the p^-/p^+ epi substrate, an improvement of the charge collection efficiency was quite small. The epi layer was thick ($8\mu m$ in this case) enough for many electron-hole pairs to be created within this layer. The electrons created in this layer were confined inside due to the p^-/p^+ potential barrier, and eventually captured at the N^+ layer.

The influence of the buried barrier on the junction capacitance was examined. Figure 4 shows the junction capacitances of the test vehicles as a function of bias voltage. In

contrast with the HiC structure, an increase of the junction capacitance due to the buried barrier was relatively small. A small increase of the junction capacitance and its flat dependence on bias voltage beyond 5V reflect that an extension of the depletion layer is limited by the tail of the buried barrier. The increase of the bit line capacitance was measured to be less than 10% in the 1Mbit DRAM. Other electrical characteristics, such as junction breakdown, leakage current and body effects of MOS transistors, were not affected by the buried barrier.

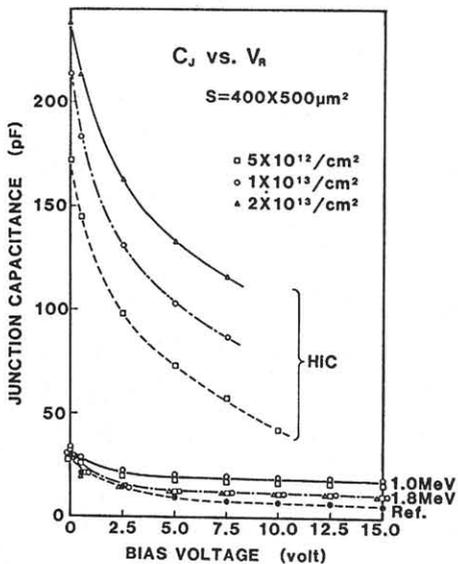


Fig.4 Junction capacitance of N+/p junction with buried barrier and HiC structure.

3. SER REDUCTION IN 1MEGABIT DRAM

The SER of the 1Mbit NMOS DRAM having a structure shown in Fig.1 was examined. The SER was measured by an accelerated test with 241Am alpha-particle source, and the estimated SER in FIT was derived by assuming an alpha-particle flux of 0.001particle/cm².hour. Figure 5 shows the estimated SER as a function of cycle time. In this case critical charge was 72fC. The buried barrier reduced the bit line mode SER (cycle time range <10us) by a

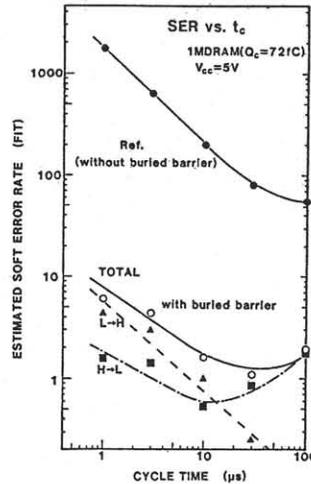


Fig.5 Estimated SER as a function of cycle time. SER was measured by an accelerated test with 241Am, and converted to SER in FIT by assuming an alpha-particle flux of 0.001particle/cm².hour.

factor of more than X100, and also the cell mode SER (cycle time range >10us) by a factor of X50 compared with the HiC structure. Figure 6 shows the estimated SER of the 1Mbit DRAM with the buried barrier as a function of critical charge. The critical charge of 60fC was found to be sufficient to achieve the SER of less than 100FIT even at a cycle time of 1us. This implies that to obtain the SER of less than 100FIT, a storage capacitance can be reduced to around 24fF at 5V operation with the aid of the buried barrier.

Further the collected charge was measured by using a test vehicle with 12K memory cells array. The memory cell is the same one as used in the 1Mbit DRAM. The accelerated SER is plotted as a function of the collected charge in Figure 7. The substrate bias voltage (VBB) dependence of the SER in an unimplanted 1Mbit DRAM is also shown in Figure 7. Figure 8 shows the estimated SER as a function of the depletion layer width. The depletion layer width was calculated by MIPS (Mitsubishi Impurity Profile Simulator) and MIDSIP (Mitsubishi Device Simulation Program). Figures 7 and 8 imply that the MeV-boron implanted buried barrier suppresses an extension of the depletion layer under the bit line N+ region, so that the charge collection

efficiency is reduced and results in improving SER.

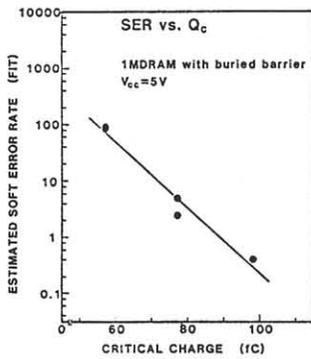


Fig.6 Estimated SER as a function of critical charge at cycle time of 100 ns.

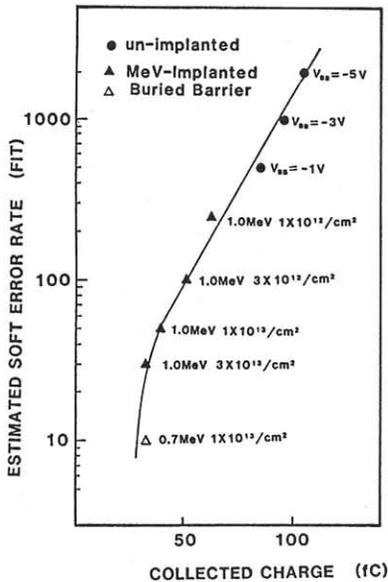


Fig.7 Estimated SER as a function of collected charge measured at bias voltage of 8V.

4. CONCLUSIONS

In applying the buried barrier to the 1Mbit DRAM, the bit line mode SER was improved by a factor of more than X100 and the cell mode SER was also reduced by a factor of X50 compared with the HiC structure.

Thus it is confirmed that the MeV-boron implanted buried barrier structure is quite effective in reducing the SER, especially the bit line mode SER, which could not be achieved by other structural modifications so far, as well as a cell mode SER. This structure has other significant advantages, they are easier threshold voltage control of transistors than other structures such as a well structure

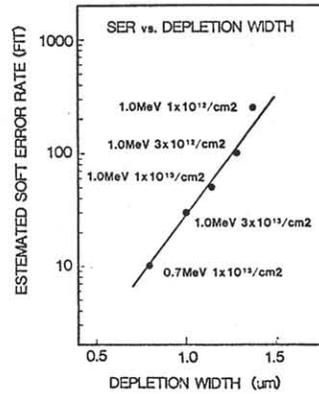


Fig.8 Estimated SER as a function of simulated depletion width at bias voltage of 8V.

(memory cell is in a relatively heavily doped well) (4) or a bit line shielded structure (only bit line N+ region is covered with p+ region) and a small increase of the junction capacitance at the bit line contact N+ region. A buried barrier formation by an MeV-implantation can be easily implemented for other type of memory cells, such as a trench type and a stacked type. With the aid of the buried barrier the SER of less than 100FIT would be achieved in megabit DRAM with the storage capacitance of 24fF at 5V operation. These results indicate that the MeV-boron implanted buried barrier structure will become a powerful candidate as a countermeasure of the soft errors in next generation DRAM's.

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