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# Initial Stage Degradation Mechanism in Hot-Carrier Effects

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The degradation of MOSFET under extremely short time stress, down to 1μsec, was investigated. This investigation makes it possible to identify fundamental processes in the device degradation. The degradation was found to have two phases. In the first phase (1μsec<t<1msec), an $I_{SUB}$ peak condition gives the largest degradation. It is caused by the creation of interface traps and by the electron trapping. In the second phase (t>1msec), the electron trapping in the oxide under an $I_G$ peak condition dominates the total degradation. The $g_m$ degradation in n-channel devices is the severest under an $I_{SUB}$ peak condition. It is caused by the hole injection which creates the interface traps.

## 1. Introduction

It is now well established that device degradation due to hot-carrier effects can be examined with a long time stress test[1)2)3)]. Carrier trapping in oxides and the creation of interface traps are believed to be the main causes of the degradation. But it is rather difficult to separate these two phenomena in the long time stress experiments. Here, the "long time" is approximately of the order of $10^0$ to $10^5$ seconds. There are several approaches to clarify the degradation mechanism. The pulsed stress experiments have given us information about the effect of carrier detrapping[4)]. In addition, the investigation of device degradation under extremely short time stress is expected to give us new information. In particular, it might be able to separate these two phenomena, because they may have time constants with different orders of magnitude.

In this paper, the degradation under extremely short time stress is investigated experimentally from the viewpoints of bias conditions and carrier types, and new findings of the degradation mechanism are reported.

## 2. Experimental

Two separate pulses with the identical pulse width were applied on both the gate and drain electrodes simultaneously with the use of the burst mode in an HP8160A pulse generator. The pulse width was varied from 1μsec to 700msec, and each pulse was followed by measurements of device characteristics ( $V_{th}$ and $g_m$ ). The time sequence is shown in Fig.1. This variable-width single pulse (VSP) technique was introduced in order to avoid AC stress effect which may have frequency, pulse rise/fall time, and gate/drain pulse timing dependence[4)]. After the accumulated stress time reached 1 second, the DC power supply was used for applying stress on the devices.

The devices used in this study were 1)p-channel single drain (SD) devices, 2) p-channel LDD devices, and 3) n-channel LDD

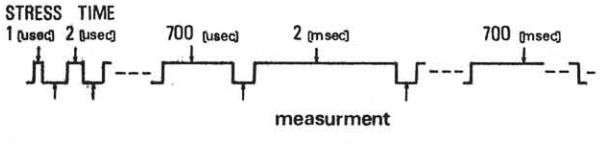


Fig.1, Time sequence of the measurement in the VSP technique.

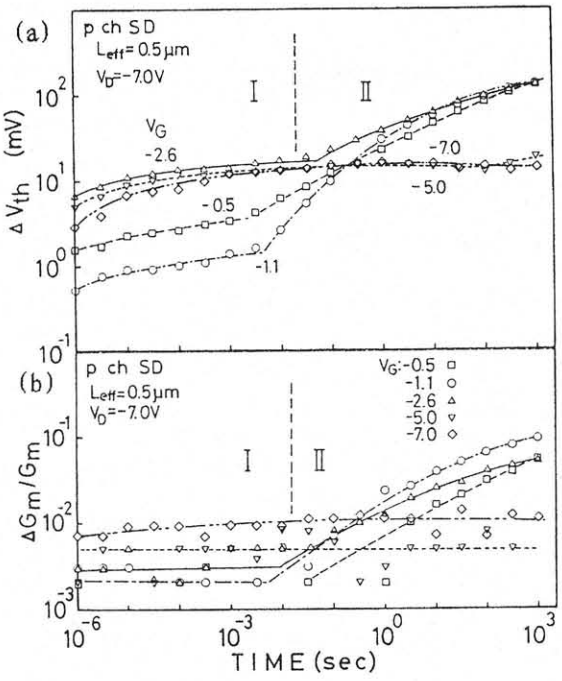


Fig.2, Degradation vs. stress time in p-channel SD devices.(a)$V_{th}$ shift, (b)$g_m$ increase.

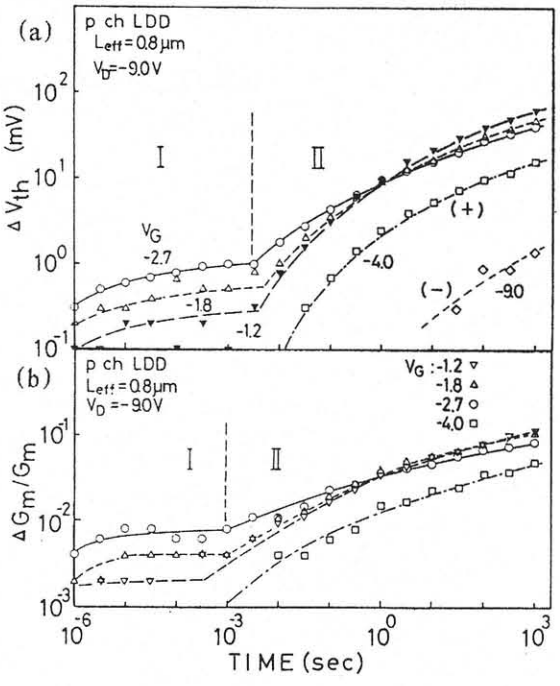


Fig.3, Degradation vs. stress time in p-channel LDD's.(a)$V_{th}$ shift, (b)$g_m$ increase.

devices with low $n^-$ doping concentration ($1\times10^{12}cm^{-2}$). They all show fast initial stage degradation[5].

## 3. Results and Discussions

In Fig.2 and 3, $V_{th}$ shift and $g_m$ degradation in both p-channel SD and LDD devices from 1μsec to 1000 seconds are shown. Here, $V_D$ is equal to -7V and -9V, respectively. It can easily be seen that the degradation has two phases. Mechanisms of these phenomena will be discussed hereafter.

### 3.1 $I_{SUB}$ peak vs. $I_G$ peak in PMOSFET

The $V_{th}$ shift has two phases. In the first phase (1μsec<t<10msec), it tends to saturate quite rapidly($\tau$<10μsec) and keeps increasing very slowly up to about 10msec. In the second pnase (t>10msec), a new degradation mode appears and dominates the degradation. In Fig.4, the time evolution of the $V_{th}$ shift is shown as a function of stress gate voltage. The corresponding $I_{SUB}$ and $I_G$ are also shown.

In phase I, the $V_{th}$ shift is the severest under the bias condition which gives the maximum substrate current. In this condition, many holes and electrons exist near the Si-

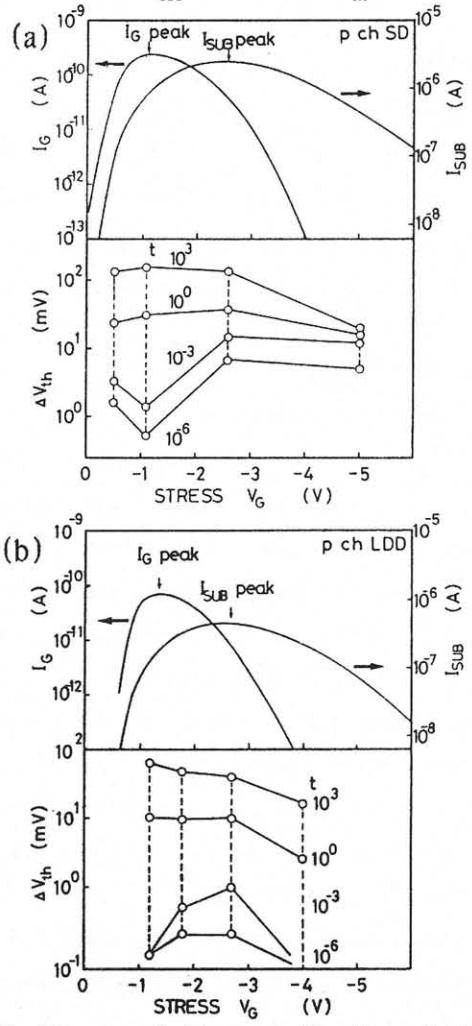


Fig.4, Time evolution of the $V_{th}$ shift and the corresponding $I_{SUB}$ and $I_G$. (a)p-channel SD devices, (b) p-channel LDD devices.

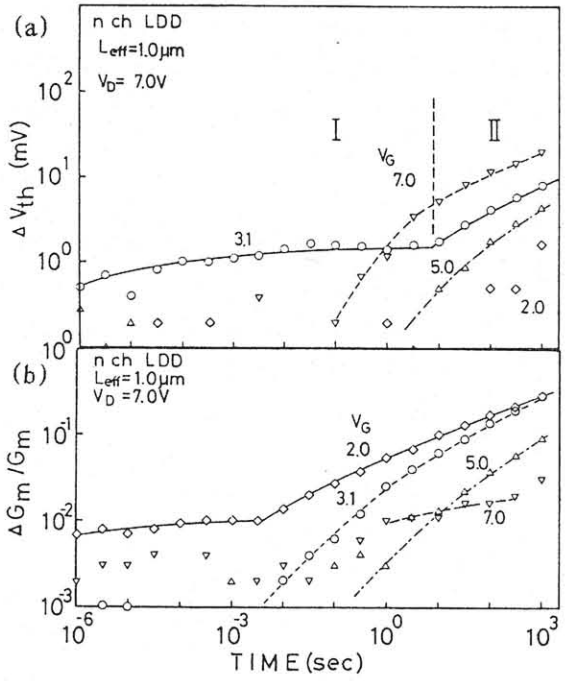


Fig.5, Degradation vs. stress time in n-channel LDD's. (a) $V_{th}$ shift, (b) $g_m$ degradation.

$SiO_2$ interface, which causes the interface trap generation and electron trapping by these traps. Since this phenomenon occurs in the region close to the interface, it might have rather short time constant.

In phase II, on the other hand, an $I_G$ peak condition gives the largest $V_{th}$ shift. Since the number of injected electrons in this case, is at a maximum, the electron trapping in the oxide traps might be the main cause of the degradation. This process might occur in the entire oxide layer, and might have a longer time constant.

The $g_m$ variation (In fact, it is a $g_m$ increase) seems to show almost the same characteristics as $V_{th}$ shift (Fig.2(b)). The $g_m$ degradation is due to the electron trapping by the interface or oxide traps.

3.2 $I_{SUB}$ peak vs. $I_G$ peak in NMOSFET

In Fig.5, $V_{th}$ shift and $g_m$ degradation in n-channel LDD devices are shown. Here, the drain voltage is 7V. $V_{th}$ shift shows the similar characteristics as that of p-channel devices. In phase I (t<1sec), an $I_{SUB}$ peak condition gives the large $V_{th}$ shift. In phase

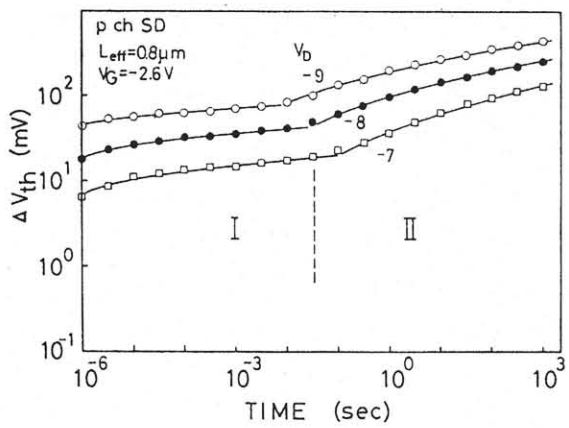


Fig.6, Initial stage degradation of p-channel devices with three different values of $V_D$.

II (t 1sec), on the other hand, an $I_G$ peak condition gives the marked degradation. This can be attributer to the fact that the electron trapping is responsible for the $V_{th}$ shift. The phase I reflects the electron trapping by the interface traps, and the phase II corresponds to the electron trapping process by the oxide traps.

$g_m$ degradation in n-channel devices is considered to be caused by the interface trap creation. The degradation in phase I corresponds to the interface trap generation by injected holes. So the lower $V_G$ condition ($V_G$=2V) gives the largest degradation. In the phase II, on the other hand, the degradation is caused by the interface trap generation by holes as well as electrons[6]. So the $I_{SUB}$ peak condition gives the largest degradation.

3.3 Electrons vs. holes

As has already been seen, this study clarifies the roles which electrons and holes play in the degradation process. Electrons are trapped by the interface traps or oxide traps, and they cause the $V_{th}$ shift in both n-channel and p-channel devices. Electron trapping is also the main cause of the $g_m$ increase in p-channel devices.

Injected holes, on the other hand, play an essential role in the trap creation, and this results in the large $g_m$ degradation. In Fig.6 is shown the initial stage degradation

with the same $V_G$ but with three different values of $V_D$ in p-channel SD devices. All are under $I_{SUB}$ peak condition. The saturated value of $V_{th}$ shift in phase I increases with $V_D$. This fact implies that the degradation in phase I is not simply the electron trapping by the interface traps which existed from the beginning. Rather, it is a compound process of interface trap generation due to injected holes and electron trapping by these created traps. In the case of n-channel devices, hole injection without electrons ($V_G$=2V) creates interface traps rapidly ($g_m$ degradation in phase I). The injection of both holes and electrons causes the severest $g_m$ degradation. The existence of both types of carriers might be responsible for the creation of the traps in the oxide, and this process may have rather long time constant. This corresponds to the usual long time stress experiments.

## 4. Conclusions

The initial stage degradation in submicron MOS devices was investigated experimentally by using the variable single pulse method. It was found that the degradation has two phases. These two fundamental processes were distinguished and characterized as follows.

1) In p-channel devices:
   First phase; Interface traps are created and electrons are captured by these traps. This process has a rather short characteristic time constant. $I_{SUB}$ peak condition gives the largest degradation.
   Second phase; The electron trapping by the oxide traps dominates the degradation. $I_G$ peak is the severest condition in this phase.
2) In n-channel devices:
   $V_{th}$ shift is caused by the electron trapping. $g_m$ degradation is caused by the interface traps created by the injected holes and electrons.

In this study, stress time down to 1μsec was examined. It has been restricted due to experimental configurations. Further investigation under stress time shorter than 1μsec is strongly expected, since it might give us deeper physical understandings about the device degradation mechanism.

The new method proposed in this study may be of great help in developing high quality insulators, or in clarifying the instability of composite insulating layers. Moreover, if combined with the Single Electron Trapping phenomenon[7], this method may clarify the physics of interface trap generation.

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