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# Effects of Parasitic Resistance and Hot-Electron-Degraded Transconductance on Lower Submicron P and N-MOSFET Characteristics

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A way to predict MOSFET parasitic resistance quantitatively, considering the device structure dependence, is presended. Using this method, the difference in parasitic resistance between buried and surface channel pMOSFET is clarified.

These differences are shown to result in different transconductance degradation behaviors due to hot-electron stress between buried and surface channel pMOSFETs.

As a result, the increase in transconductance degradation for surface channel pMOS is not so extreme as that within the acceptable level.

## I. INTRODUCTION

Parasitic resistance and device characteristics degradation effects, due to hot carrier stress, are becoming more important issues for MOSFETs as device miniaturization continues. Especially for pMOSFET, it is becoming urgent to determine which structure, buried or surface channel, is suitable under the condition of device miniaturization.

As there have been no quantitative predictions of parasitic resistance[1], considering the device structure dependence, many things have remained unclear, according to the quantitative comparison between buried and surface channel pMOSFETs. Furthermore, regarding device characteristics degradation due to hot carrier stress, no clear model exists for pMOSFET, as exists for nMOSFET[2].

This paper reports results of study on the difference on parasitic resistance between buried and surface channel pMOSFETs, using 2D device simulation. Then, the authors clarified that such parasitic resistance characteristics make the different behavior for characteristics degradation in both pMOSFETs structures.

## II. PARASITIC RESISTANCE

While Ng's calculations[1], based on the analytical model, have been proposed to date, with the device miniaturization it is becoming more critical to predict the source・drain parasitic resistance quantitatively. So this paper presents the simulation method to deal with the parasitic resistance, based on the distribution of quasi-Fermi potential and considering the structure dependence.

In Fig.1, the shape differences in the depletion region, between surface and buried channel MOSFETs, is shown. These differences result in different behavior for series resistance, as shown in the equivalent circuit model in Fig.1. The point is that, in buried channel case, accumulation resistance Rac does not exist and only spreading resistance Rsp compose the series resistance.

FIg.2 shows simulated parasitic resistance

$R_{SD}$ for both surface and buried channel pMOSFETs, as a function of a gate bias Vg. Also experimental results[3] are shown. Agreement between simulated and measured results is rather good, except for the buried channel on the low Vg region, where Rch increases significantly, so that dividing experimentaly a small $R_{SD}$ value from a large Rch value inevitably involves measurement error.

For the surface channel, monotonic $R_{SD}$ increase is observed, with the decrease in Vg. In buried channel case, no rapid $R_{SD}$ increase is observed and, at low gate bias region, the increase saturates.

The reason for this difference is that, in the case of a buried channel, Rac does not exist and the current spreading point does not move, different from a surface channel case, while with the Vg decrease the current flow spreads so that Rsp is saturated.

The parasitic resistance effects on scaled down MOSFETs are evaluated for various structures in Fig.3. For supply voltage, $1/\sqrt{k}$ (k:scaling factor), reduction is chosen, so that the maximum internal electric field is conserved constant and the hot-carrier effect is also scaled down.

It can be seen that $R_{SD}$ decreases for all structures, except for LDD nMOSFET, as well as Rch with channel length Lc miniaturization.

This $R_{SD}$ feature is important[1], because, even if the other parasitic resistance components, such as sheet resistance Rsh and contact resistance Rco increased, the total parasitic resistance does not increase.

## III. DEGRADATION DUE TO HOT-ELECTRON

In this section, the hot-electron stress effect on surface and buried channel pMOSFETs is discussed. In the case of nMOS, transconductance degradation[2] is due to the increase in parasitic resistance in the depleted region, which is induced under the trapped electrons. However, for pMOS, a quantitative model and discussion, corresponding to the above model for nMOS, has not yet been reported.

Fig.4 shows Rch and $R_{SD}$, before and after stress, as a function of Vg. Here, it is assumed that the same charge density is trapped on the source side (reverse mode mesurement) for both surface and buried channel pMOS.

It can be seen that, in the case of pMOS, $\Delta$Rch (modulation (reduction) of Rch) is extremely larger than $\Delta R_{SD}$ (modulation of $R_{SD}$), showing that the resistance modulation extends over a rather wide region, on the contrary to the case of nMOS. $\Delta$Rch is larger for a buried channel than for a surface channel. Although the $\Delta R_{SD}$ is nearly the same amount for both cases, for buried channel pMOS, Vg dependence of $R_{SD}$ is modified after stress, showing that additional resistance components are created due to hot-electron stress.

Now, $R_{TC}$, the resistance component modulated by trapped charge, is introduced.(Fig.5) After stress, it is considered that the parts of Rch and $R_{SD}$ which locate under the trapped electrons, is modulated to $R_{TC}$, low resistvity accumulation resistance.

For buried channel pMOS, from Fig.4, it can be seen that $\Delta$Rch($\sim$1k$\Omega$)is about 20 times larger than $\Delta R_{SD}$ ($\sim$0.05k$\Omega$) at Vg=-1v. From these relations, $R_{TC}$ is estimated as $R_{TC} \sim 0.2k\Omega$ and nearly the same amount of pre-stress $R_{SD}$. Furthermore, in the case of a buried channel, as mentioned previously, pre-stress $R_{SD}$ is composed only of spreading

resistance Rsp and the following relation is finally obtained, where

$R_{TC} \sim Rac \sim Rsp$ .

As Rac is almost inversely proportional to accumulated charge Nac, Nac is estimated as

$Nac \sim 3x10^{12}\ cm^{-2}$ .

This is consistent with trapped charge density $N_{TC} \sim 1x10^{12}\ cm^{-2}$ .

For a surface channel pMOSFET, however, pre-stress series resistance already involves accumulation resistance Rac . Therefore, compared to the previous buried channel case, the resistance modulation in the surface channel is smaller.

These differences in the hot-electron stress effects on buried and surface channels are shown more clearly in Fig.6. Fig.6 shows the degradation in a transconductance $\Delta gm$ and a threshold voltage $\Delta Vth$ as a function of the trapped charge density.

A $\Delta gm$ comparison shows that the amount of transconductance degradation for a buried channel pMOS is largest, followed by that for LDD nMOS and surface channel pMOS, in order of magnitude.

Therefore, consistent with the difference in degradation mechanism mentioned previously, the surface channel pMOS structure may be less affected by the trapped electrons, on transconductance degradation, compared to a buried channel pMOS.

Therefore, it is concluded that the transconductance degradation in a surface channel pMOS would be on a acceptable level. On the other hand, according to the threshold voltage degradation, the buried channel shows an extremely larger amount of degradation than the surface channel. This degradation is more severe with device miniaturization.

## VI. CONCLUSION

The parasitic resistance difference, between buried and surface channel pMOSFETs, are shown to result in the different behavior of transconductance degradation due to hot electron stress. As a result, the increase in transconductance degradation for surface channel pMOS is not as extreme as that within the acceptable level.

So, considering the excellent performance of surface channel pMOS, with the device miniaturization to a sub-half-micrometer, surface channel pMOS would become a suitable structure.


References

1)K.Ng and W.Lynch ED-33,965('86), ED-34,503('87)

2)F.Hsu and H.Grinolds EDL-5,71('84)

3)T.Noguchi et.al. IEDM ('86)730


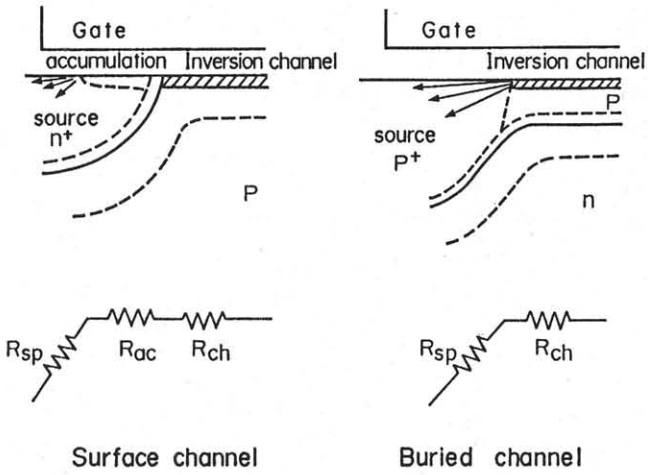


Fig.1 Depletion region shapes for surface and buried channel MOSFET, both at built-in and biased state. Coresponding parasitic resistance components represented as equivalent circuit models.

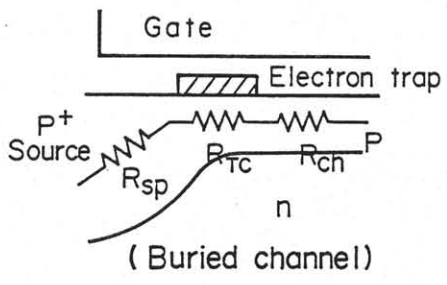


Fig.5 post-stress parasitic resistance components, shown as a equivalent circuit model

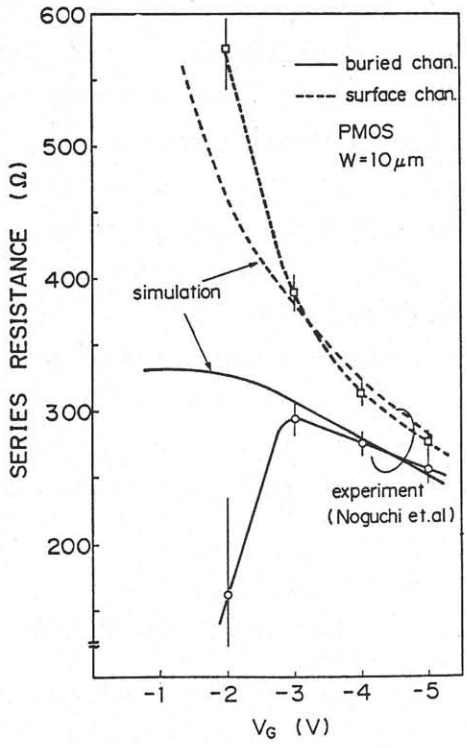


Fig.2 Simulated and measured (Noguchi et. al.[3]) parasitic resistance for both buried and surface channel pMOSFETs as a function of gate bias Vg.

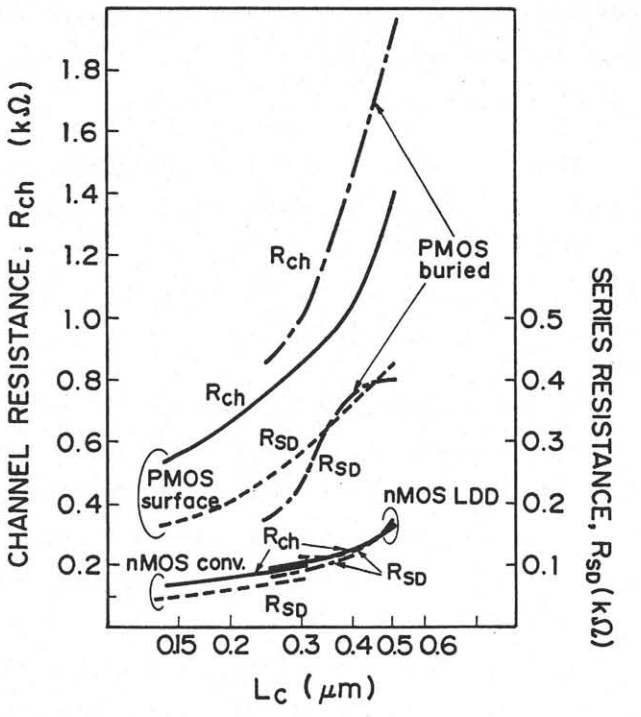


Fig.3 Channel resistance Rch and parasitic resistance $R_{SD}$ for various MOSFET structures, as a function of channel length Lc.

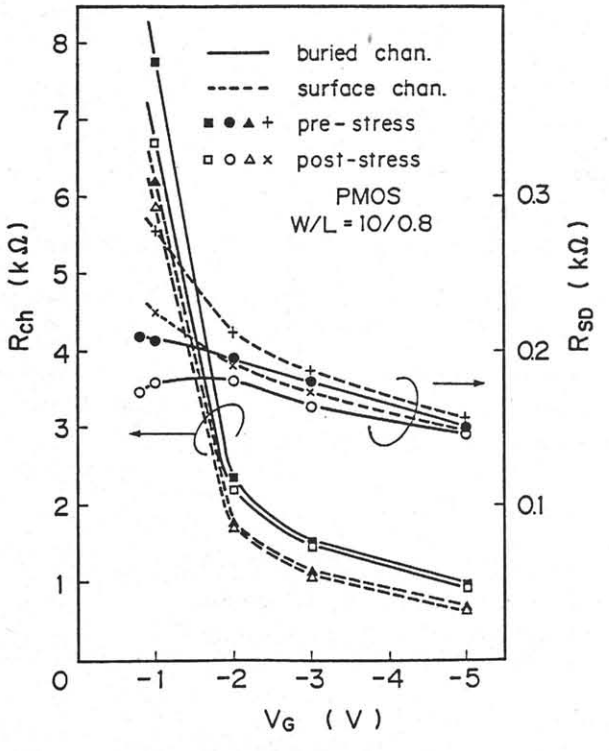


Fig.4 Channel resistance Rch and parasitic resistance $R_{SD}$, before and after stress, as a function of gate bias Vg.

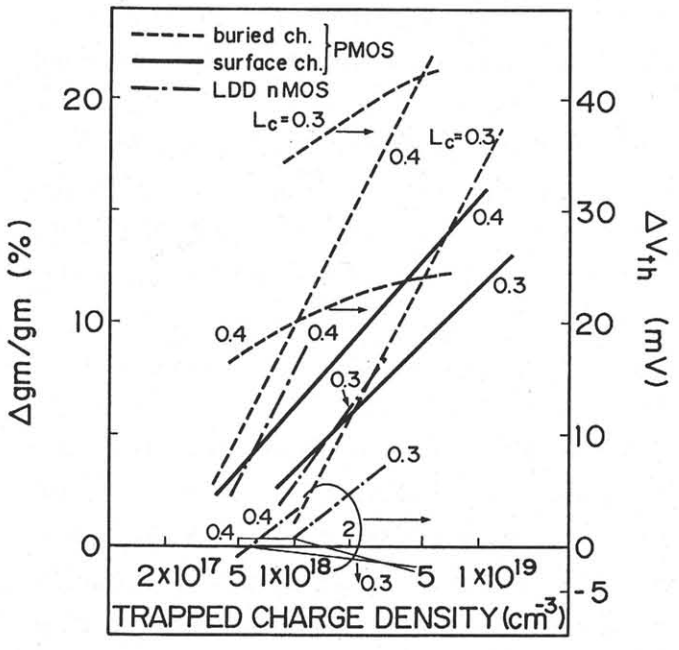


Fig.6 Degradation of a transconductance gm,max and a threshold voltage Vth for various MOSFET structures (channel length Lc: 0.3 and 0.4 μm), as a function of the trapped charge density.