Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 51-54

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Vertical-Type Amorphous-Silicon MOSFET IC's

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High performance vertical-type amorphous-silicon (a-Si) MOSFET have been demonstrated for the first time. Field-effect mobility was 1.1 cm^2/Vs. A seven-stage E/E type ring oscillator has been fabricated by using the vertical-type a-Si MOSFET. The minimum propagation delay time was 95ns/stage. RS flip-flop circuit was also evaluated.

I. Introduction

Amorphous-silicon field-effect transistors (a-Si FET's) have been investigated extensively for large area switching devices, such as matrix-addressed panel-displays[1] and contact-type image sensors[2]. The most serious shortcoming of the present a-Si FET's is of their low operation speed due to low field-effect mobility of electrons in a-Si. Many researchers have demonstrated a-Si logic circuits by using the conventional FET structure[3,4], but their operation speeds were far from the minimum value necessary for practical circuits. In order to attain the practical circuit operation, i.e., MHz-rate operation, transit time of electrons in a-Si FETs should be drastically shorten by reducing their channel length by an order in magnitude, because the transit time of electrons is inversely proportional to square of the channel length.

We have proposed a novel vertical type a-Si FET[5,6] whose channel length can be easily reduced to submicron region since it is not delineated by photoetching process.

In this paper, we have presented high performance vertical-type a-Si MOSFETs and their circuit operation.

II. MOSFET Fabrication Process

There are two key demands in fabricating high performance vertical-type a-Si FETs. They are 1) satisfactory good electrical properties at the insulator/a-Si interface and 2) negligibly small parasitic capacitance and resistance. We have shown that the second demand can be satisfied by using the self-alignment technology by using reactive ion etching (RIE) technique and by introducing highly conductive source and drain of microcrystal silicon (μc-Si). In this paper, the previously mentioned first demand has been satisfied by applying low-temperature thermal oxidation technique[7].

Fabrication steps of the vertical-type a-Si MOSFET are almost similar to those reported in the previous letter[6]. In order to introduce low-temperature thermal oxidation method to the vertical-type a-Si

FET, however, we applied Cr/Ta double layer as the top electrode. The top Cr layer was chemically patterned and used only as the etching mask for RIE. And the Cr layer was removed before oxidation since it is dissolved during the oxidation. Since Ta layer is oxidized easily, metal layers of Ta were covered by n^-a-Si during the oxidation.

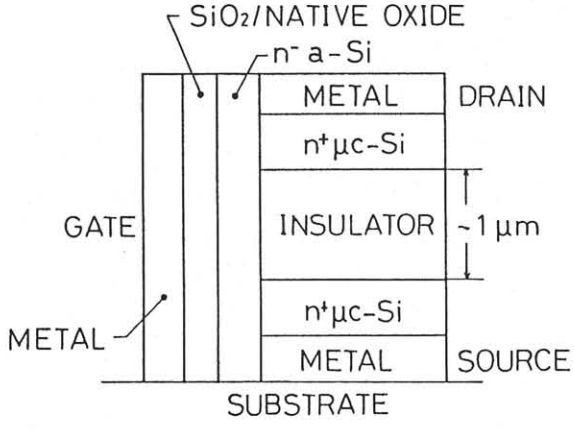

Fig.1. Cross-sectional view of the vertical-type a-Si MOSFET.

Cross-sectional view of fabricated vertical-type amorphous-silicon MOSFET are shown in figure 1. The thicknesses of upper metal of Ta, n^+μc-Si, SiN, n^+μc-Si and lower metal of Ta layers were chosen as 200nm, 300nm, 1μm, 300nm and 200nm, respectively. Gate insulators of CVD SiO_2 and native oxide were 90nm and 10nm thick. Mo and Al double layers of 500nm and 1μm thick, respectively, were used as the gate electrode and interconnection lines. Since offset voltage was decreased and field-effect mobility was increased with the decrease of the active n^- layer thickness, active layer was chosen to be as thin as 80 nm.

III. FET Performance.

Typical FET characteristics with only 10nm thick native oxide gate are shown in figure 2. Drain current started to increase linearly with drain voltage and showed clear saturation characteristics since parasitic resistances in source and drain are very low.

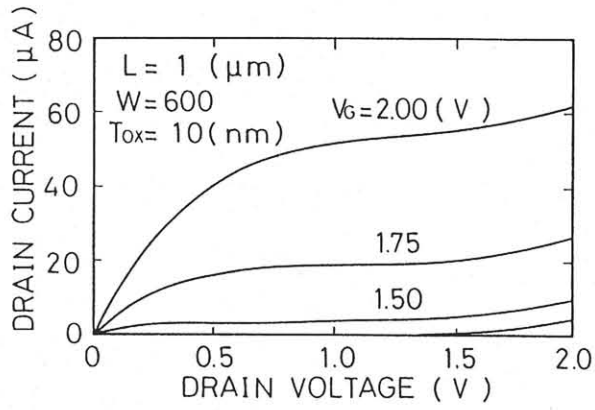

Fig.2. Linear I_D-V_D characteristics of the vertical type a-Si MOSFET with native oxide gate.

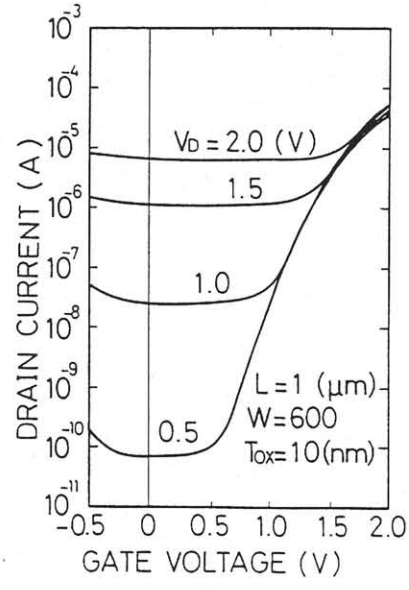

Fig.3. Semi-logarithmic I_D-V_G characteristics of the vertical-type a-Si MOSFET with native oxide gate.

Threshold voltage was about 1.3V. Field-effect mobility under low field conditions was 1.1 cm^2/Vs. The maximum gate and drain voltages applicable were less than 2V because of gate insulator breakdown. Thus high voltage operation and high speed operation is possible only for the FET with additional CVD SiO_2 gate.

Figure 3 shows semi-logarithmic drain current as a function of gate voltage. Large on/off current ratio was obtained under low V_D conditions. However, ON/OFF current ratio at V_D=2V was less than 10. This value is much smaller than the one necessary for matrix

addressed panel displays and peripheral circuits.

There are three possible origins of large leakage current under high V_D conditions. They are 1) hole conduction, i.e., p-channel operation at the front MIS interface, 2) bulk space charge-limited current (SCLC), 3) electron conduction induced by back gate effect of drain through thick SiN layer. Since the current did not increase sharply at the negative gate voltage, the hole conduction seems not to play a dominant role. SCLC density of an n-i-n sandwich structure with the 1μm thick n^- layer was about 10 mA/cm^2 at 2V bias voltage. While, average current density flowing the active region of the FET biased at V_G=0 and V_D=2V was about 13 A/cm^2, which is much higher than the SCLC value. SCLC seems also not to play a dominant role and thus, we concluded that the back gate effect is the most important for large leakage current and should be suppressed in the future.

IV. Circuit Performance

Integrated E/E inverter circuit has been evaluated. The channel width of the driver and load of vertical-type MOSFET with a native oxide gate were 600μm and 60μm, respectively. The channel length was 1μm. The transfer curves for various gate voltage V_{GG} of the load FET are shown in figure 4. Drain voltage V_{DD} of load transistor was fixed at 2V. Clear logical "NOT" operation was obtained. Maximum small signal gain was 1.7.

Microscopic photograph of seven-stage ring oscillator by using the similar inverter is shown in figure 5. Long and narrow white stripes were not of the channel region but of the 20μm wide upper Ta layer. Channel is formed at the side wall of the stripe.

Figure 6 shows relation between power dissipation per gate and propagation delay time evaluated by ring oscillator. Upper-left characteristics are of those from the FET with only 10nm-thick native oxide gate and lower-right characteristics are of those from the FETs with CVD SiO_2/native oxide double-gate structure. Drain voltage of load transistor V_{DD} was 2 and 20 V for the native oxide gate FET and double-gate FET, respectively. The minimum propagation delay time of 95ns/stage was attained when V_{DD}=20V and V_{GG}=50V. This value is about two times shorter than that of E/R circuit reported by Hiranaka et.al.[4]. But this propagation delay is five times longer than the value expected by using mobility (0.5cm^2/Vs) and capacitance

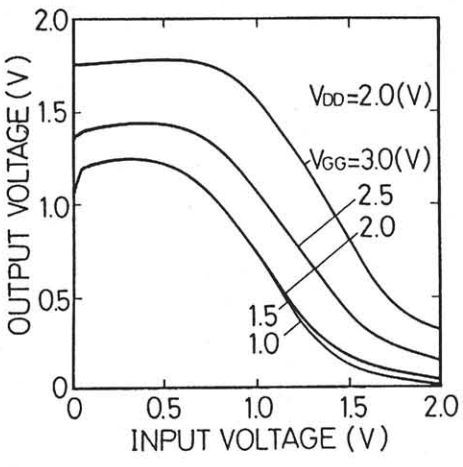

Fig.4. The transfer characteristics of the E/E type inverter formed by a-Si MOSFET with native oxide gate for various V_{GG} values.

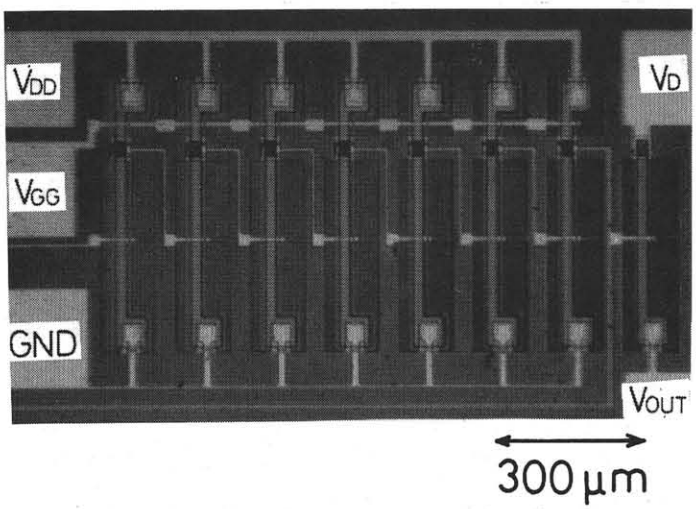

Fig.5. The microscopic photograph of a seven-stage ring oscillator.

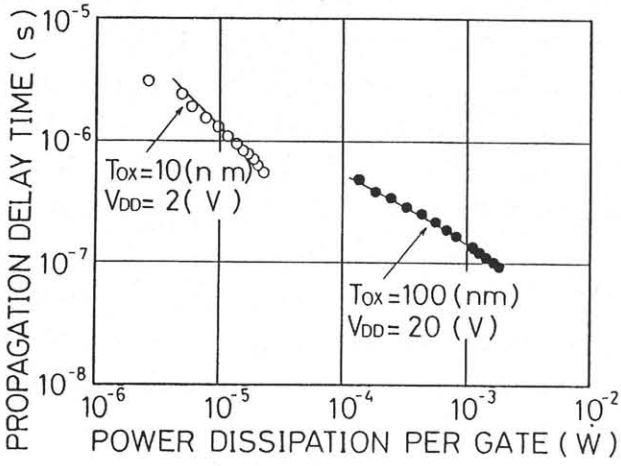

Fig.6. Relation between power dissipation per gate and propagation delay time of seven-stage ring oscillator.

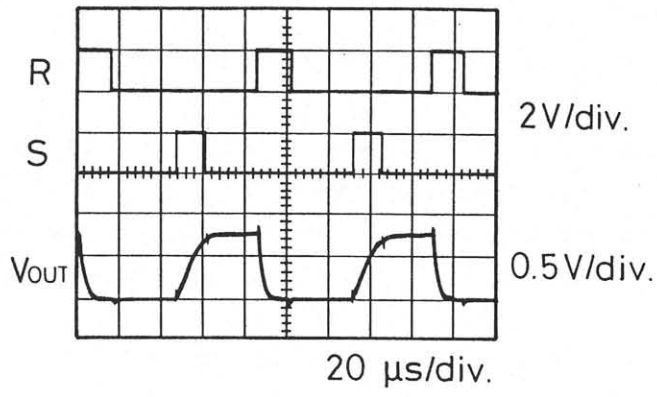

Fig.7. Response waveforms of RS flip-flop.

of double-gate FET. Power delay product was 13pJ for native oxide gate FET and 170pJ for double-gate FET, respectively. The latter is one order an magnitude larger than the former because these value is proportional to gate capacitance multiplied by V_{DD} squared.

RS flip-flop of NOR configuration were fabricated by using the FET with native oxide gate. Reset and set signals of non-overlapping 2V clock pulse were applied to the driver FET gates. V_{DD} was kept at 2V and V_{GG} was 4V. Response waveforms are shown in figure 7. Clock frequency was 12.5 kHz. Output waveform V_{OUT} was raised when set pulse is applied and V_{OUT} was fallen when reset pulse is applied. Since rise time was about 12µs, Set/Reset operation seems possible at 50 kHz.

V. Conclusion

Vertical type a-Si MOSFET IC have been fabricated and investigated for the first time. The minimum propagation delay time of 95ns/stage has been achieved by a proto-type ring oscillator. Superior circuit performance will be attained by optimizing the device structure and circuit configuration.

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