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Peripheral Drive Circuits for Poly-Si TFT LCD

J. OHWADA, M. TAKABATAKE, H. KAWAKAMI, Y.A. ONO, A. MIMURA,
K. ONO, N. KONISHI, T. SUZUKI, AND K. MIYATA

Hitachi Research Laboratory, Hitachi, Ltd.
Hitachi, Ibaraki 319-12, Japan

New types of peripheral drive circuits for high resolution active matrix liquid crystal displays have been fabricated by low temperature processed poly-Si TFTs on glass substrates. Sufficient drive ability is obtained by test circuits made by n-channel enhancement type poly-Si TFTs: The maximum clock frequency of scan drive circuits is 100kHz, and in the data drive circuits one bit data signal is found to be addressable within 0.16μs.

1. Introduction

Recently interests in poly-Si thin film transistor (TFT) addressed liquid crystal displays (LCDs) are increasing, especially in low temperature processed poly-Si TFTs deposited on glass substrates. These poly-Si TFTs have a high field effect mobility of more than 30 cm^2/Vs, so that realization of large area and high resolution displays becomes possible.[1] Furthermore, peripheral drive circuits can be integrated so that number of external drive LSIs and external connections can be reduced drastically. Therefore low price and compact TFT LCDs should be realized in the near future.

Peripheral circuit integration in a high temperature processed poly-Si TFT LCD was reported by Morozumi et al.,[2] where scan and data drive circuits were integrated in a 1.51" diagonal display. Oana[3] reported on scan drive circuit integration by low temperature processed poly-Si TFT on a 1.7" diagonal display. However, large size and high resolution displays with integrated peripheral circuits are required for VDTs in OA application, such as personal computers and word processors. To realize these peripheral circuits, new types of drive circuits are necessary.

In the present paper, we describe newly developed peripheral circuits fabricated by poly-Si TFTs on glass substrates by low temperature process technology below 600°C.

2. Characteristics of Poly-Si TFT

Figure 1 shows the drain current-gate voltage (I_D-V_G) characteristics of low temperature processed poly-Si TFT. The channel width W is 10μm and channel length L is 50μm. Poly-Si TFT characteristics are as follows: Field effect mobility is 37 cm^2/Vs and threshold voltage is 6.2V. The on/off ratio of drain current is more than 10^6.

3. Peripheral Drive Circuits

Figure 2 shows a schematic structure of a peripheral circuit integrated TFT LCD. Peripheral circuits consist of scan drive circuits and data drive circuits. Scan drive circuits are connected to gate bus lines of pixel TFTs and data drive circuits are connec-

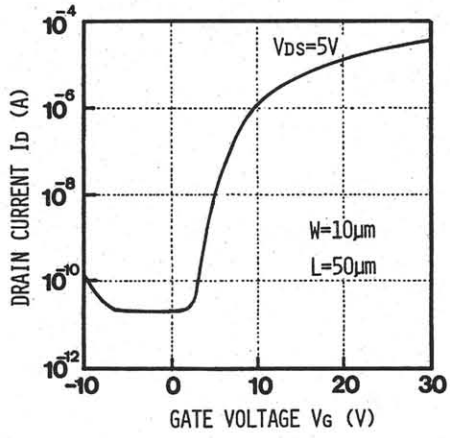

Fig.1. Drain current-gate voltage (I_D-V_G) characteristics of poly-Si TFT

ted to drain bus lines.

We have fabricated both scan test circuits and data test circuits. Characteristics of these circuits are discussed in detail.

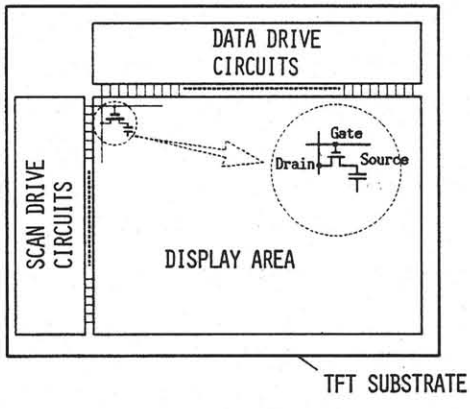

Fig.2. Schematic structure of a peripheral circuit integrated TFT LCD

3.1 Scan drive circuits

Figure 3 shows the circuit diagram of one stage and microphotograph of test circuits of five-stage scan drive circuits, which consist of shift registers, buffers, level shifters, and multiplexers. All TFTs for these circuits are of n-channel enhancement type so that fabrication of circuit TFTs can be made by the same process as that of pixel TFTs. Shift registers are of two-phase clock dynamic type and level shifters are composed of three inverters. In order to drive large load capacitance C_L of gate bus line, channel width of multiplexer is taken to be as large as 1.83 mm.

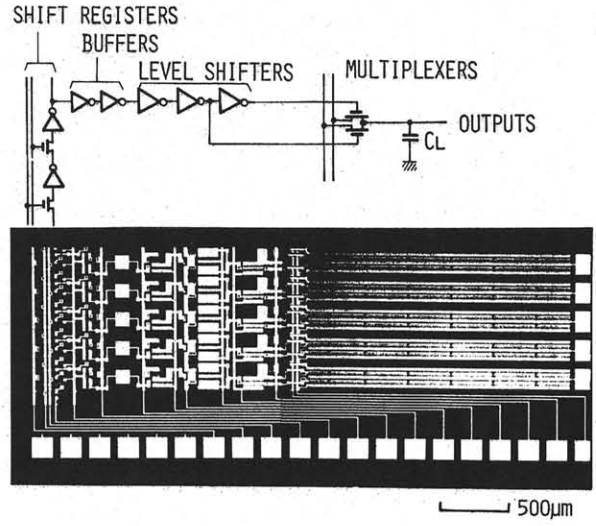

Fig.3. Circuit diagram of one stage and microphotograph of test scan drive circuits

Input voltage waveform and output voltage waveform at the 5th stage are shown in Fig.4 for two cases with clock frequency f_{CP} of 10kHz and 50kHz. Here the maximum supply voltage to level shifters is 30V and the supply voltage to multiplexer is 20V. Value of 350pF for C_L corresponds to about 2000 pixels. We note that almost the same waveforms of output voltage are obtained for all stages.

As can be seen from the graph, output voltage waveform shows fast switching behavior even at f_{CP}=50kHz: This is fast enough to drive 350pF.

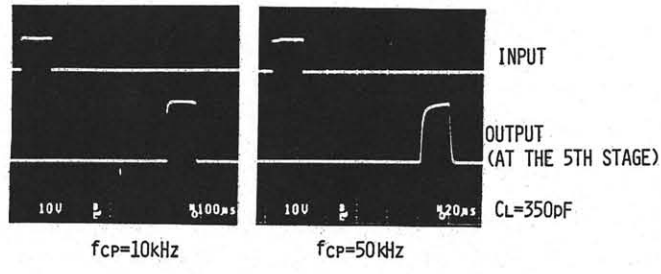

Fig.4. Input voltage waveform and output voltage waveform at the 5th stage of scan drive circuits

Figure 5 shows circuit performance of scan drive circuits in terms of output voltage vs. clock frequency characteristics. The maximum attainable clock frequency is 100kHz, much larger than 24kHz necessary to drive a 400 scan-line display at the frame frequency of 60Hz.

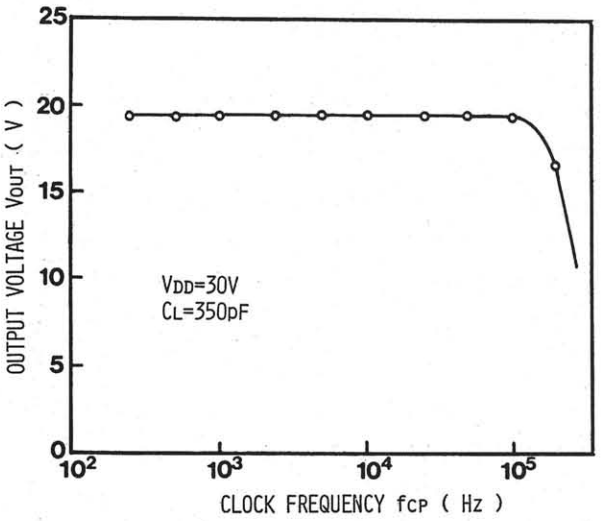

Fig.5. Output voltage vs. clock frequency characteristics of scan drive circuits

3.2 Data drive circuits

Figure 6 shows the circuit diagram and microphotograph of a test circuit of data drive circuits, which consist of divided matrix switches, line memories,inverters, and multiplexers. All TFTs for these circuits are of n-channel enhancement type. Twelve data circuits are grouped together in the divided matrix switches so that these circuits can be processed in parallel. Twelve bit data with voltage V_{DT} are stored in line memories simultaneously when the block select voltage V_B is applied to TFT gates in the divided matrix switches. One of the two TFTs in a multiplexer is selected by the output voltage of an inverter.

Figure 7 shows the drive voltage time chart for data drive circuits. This time chart describes the case that block number is k and each block consists of twelve data circuits. Period for each scan line is divided into two parts with period t_1 and t_2.

First we consider the first scan line case. First part of the scan period t_1 is divided into k parts with the pulse width t_{IN} for block select voltage: $t_{IN} = t_1/k$. In this period, twelve bit data are stored in the line memories. During the second period t_2, these data are held in line memories and output voltages are continued to be applied to all the drain bus lines of diaplay area. This procedure is repeated in all other scan lines, so that a line-at-a-time drive scheme is realized.

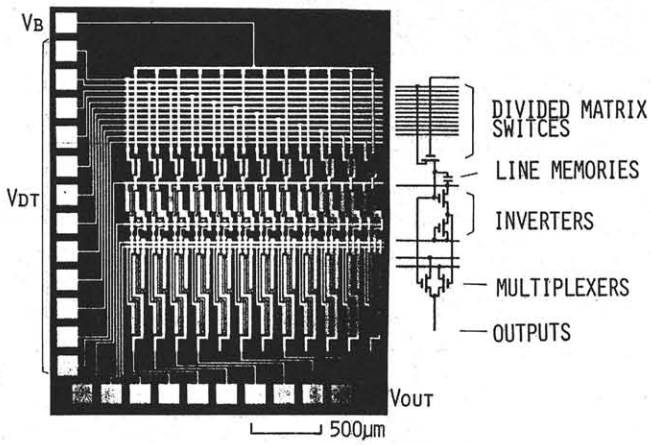

Fig.6. Circuit diagram and microphotograph of test circuit of data drive circuits

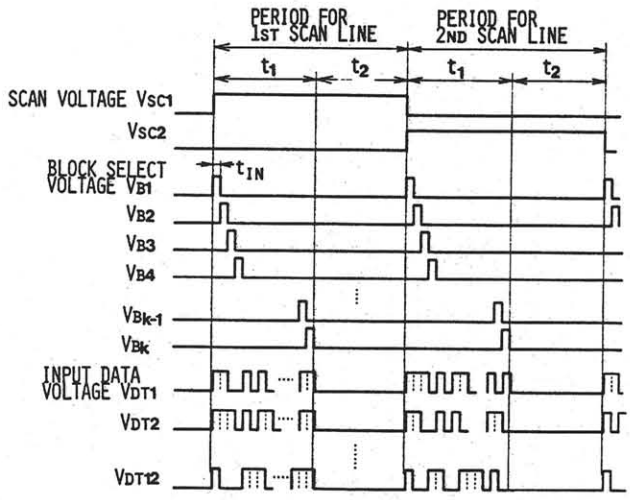

Fig.7. Drive voltage time chart for data drive circuits

Figure 8 shows an output voltage waveform together with those of block select voltage V_B and data voltage V_{DT}. The pulse width of block select voltage is 0.2 μs. The polarity of output voltage is changed in every four scan lines in order to drive a liquid crystal display. This figure indicates that output voltage levels are held during the one scan line period, 40 μs in the present case.

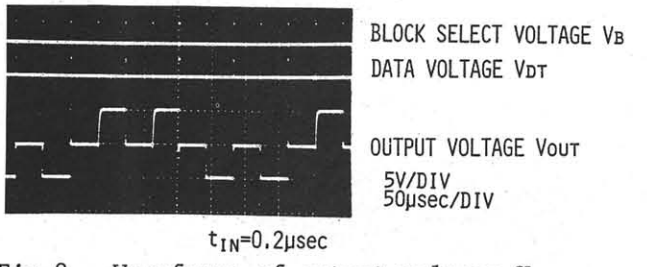

Fig.8. Waveforms of output voltage V_{OUT}, block select voltage V_B, and data voltage V_{DT}

Figure 9 shows data circuit performance in terms of output voltage vs. pulse width of block select voltage, t_{IN}. The output voltage is set at 10V in peak-to-peak value, large enough to drive liquid crystal displays. As can be seen from the graph, these data drive circuits can operate in the pulse width region down to t_{IN} = 0.16 μs, which happens to be the measuring limit of our measurement circuits.

The maximum addressable block number k ($=t_1/t_{IN}$) is estimated to be 125, since the first part of the scan period t_1 is set at 20 μs. Therefore in the case of 12 data circuit grouping in each block, the maximum addressable data line number M is 1500, while in the case of 24 data circuit grouping in each block, M becomes 3000.

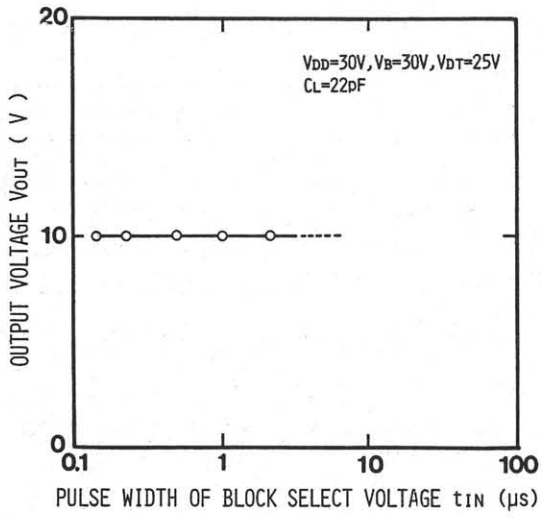

Fig.9. Output voltage vs. pulse width of block select voltage in data drive circuits

From these results, data drive circuits are found to be capable of driving high resolution LCDs, such as 640(×3)×400 dot LCDs, at the frame frequency of 60Hz.

4. Conclusions

New types of peripheral circuits for high resolution active matrix liquid crystal displays have been fabricated by low temperature processed poly-Si TFTs on glass substrates.

Sufficient drive ability is obtained by test circuits made by n-channel enhancement type poly-Si TFTs. The maximum attainable clock frequency of scan drive circuits is 100kHz, much higher than 24kHz necessary to drive a 400 scan-line display at the frame frequency of 60Hz. Data drive circuits are grouped together into blocks in the divided matrix switch scheme. The minimum addressable pulse width of block select voltage is found to be 0.16μs.

From these data, developed peripheral circuits are found to be capable of driving high resolution LCDs, such as a 640(×3)×400 dot display, at the frame frequency of 60Hz.

Acknowledgement

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3) Y. Oana, SID 84 Digest (1984) 312.