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High Performance Superthin Film Transistor (SFT) with Twin Gates

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Superthin film transistors have been studied to realize a high speed LSI. Using the twin gates structure, the field effect mobility or the carrier density in the channel increased due to the channel potential modulation. The devices show high performance, as compared to individual single gate transistors. The field induced current increased to 990 uA from 420 uA and the threshold voltage and the subthreshold slope were improved drastically in the twin gates transistor, while the gate input capacitance was nearly constant. These effects were found to show the dependence on the active layer thickness, whereby 20-70 nm was the optimum thickness.

1. Introduction

Recently, very short channel transistors have been studied to realize a high speed LSI. The short channel effect, the lowering of the field effect mobility and the increase of the threshold voltage are main problems in the devices. XMOS transistor was proposed as a candidate for the 3D IC and the short channel transistor[1]. Double-Gate thin film transistor was analized[2] and dual gate a-Si:H thin film transistor was fabricated to show the effect of the increase of the drain current.[3] On the other hand, polysilicon superthin film transistors have been studied to advance the device characteristics.[4]

This paper describes the improvement of the electrical characteristics by the effect of twin gates structre in large grain polysilicon superthin film transistors (SFT).[5] Especially, active layer thickness and the ratio of the top to the bottom gate insulator are reported to be a key factor in twin gates transistors. New SFT could be applied to ultra small size silicon transistors as well as polysilicon TFT.

2.Experiments

5-inch size Si Wafer was used as a substrate. 500nm thick oxide film was formed thermally at 1000°C. Then 150nm thick polysilicon film was chemically deposited at low pressure. The film was amorphized by implantation of Si ion at 30keV, $1.5 \times 10^{15} cm^{-2}$ and 70keV, $5 \times 10^{15} cm^{-2}$, respectively. Then solid phase recrystalization was done at 600 °C furnace for 100h. The average grain size was enlarged to about 1 um through the process.[5] In order to study the active layer thickness dependence, the polysilicon film was thinned to 20,25,35,45,70 and 105 nm by solution etching. Etch rate is 2nm/min. 50nm thick gate oxide was chemically deposited at 400°C after a transistor isolation process. Phosphorous doped polysilicon was deposited and annealed for gate electrode. Source and drain were formed by implantation of As.Al electrode was formed. The gate channel length and width were 10 um and 100um, respectively. The cross sectional scanning electron microscope photograph is shown in Fig.1. Doped polysilicon and single silicon substrate were used as the

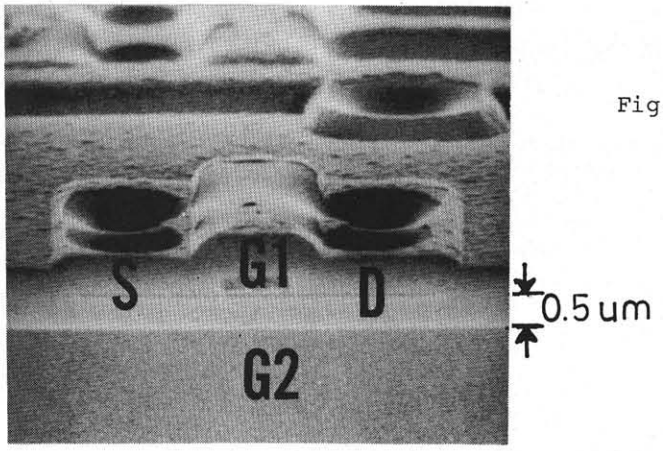

Fig. 1 Cross sectional scanning electron microscope photograph of superthin film transistor with twin gates (G1--top gate, G2--bottom gate)

top and bottom gate electrodes, respectively. The thickness of the gate insulator was 50nm for the top gate and 500nm for the bottom gate.

3.Results and Discussion

The transistors were measured by three type of bias condition. First, the top gate was used as the gate electrode and the bottom gate was connected source. Secondly, the bottom gate was used as the gate electrode and the top gate was connected to the source. Thirdly, the top and bottom gates were used as the gate electrodes. We named this as twin gates MOS transistor. Fig.2 shows the characteristics of I_{DS} vs V_{DS}. The gate voltage was chosen as follows; top gate was varied from 0 to 5V and bottom gate from 0 to 25V. This ratio was constant and 5. In the twin gates, drain current was twice as much as the arithmetic sum of the individual drain current; $I_{D(twin)} > I_{D(T)} + I_{D(B)}$. Next, we observed the thickness dependence on the increase in drain current. The measurement condition was same as the above. Fig.3 shows the results. From the figure, the maximum drain current was found at 30nm thick. More than 100nm, the drain current was nearly equal to the sum of the individual drain current. Then, the subthreshold characteristics was measured at three type condition mentioned above. As shown in Fig.4, the subthreshold slope was improved in twin gates. The characteristics of the three type of transistors was listed up in Table.1.

In our speculation, these effects were interpreted as follows. In this experiment, the bottom surface potential was weakly inverted due to the thick gate insulator and the top surface potential was inverted at the individual gate bias. When the top and bottom gates were biased simultaneously, the potential in the channel was modulated, because the surface potential was influenced mutually. That is, inversion layer induced only by the top gate was spread by the bottom gate bias. Therefore, the field effect mobility or the induced carrier increased. The drain current increased to about twice as compared to the sum of the individual drain current. These effects were not observed in the thick active layer more than 100nm, because the bottom surface potential does not influence the top surface potential. The thickness dependence on the drain current was caused by the degree which the top surface potential was modulated by the bottom gate bias.

High speed operation in LSI will be obtained by the superthin film transistor with twin gates. The device has large transconductance without the increase of the gate

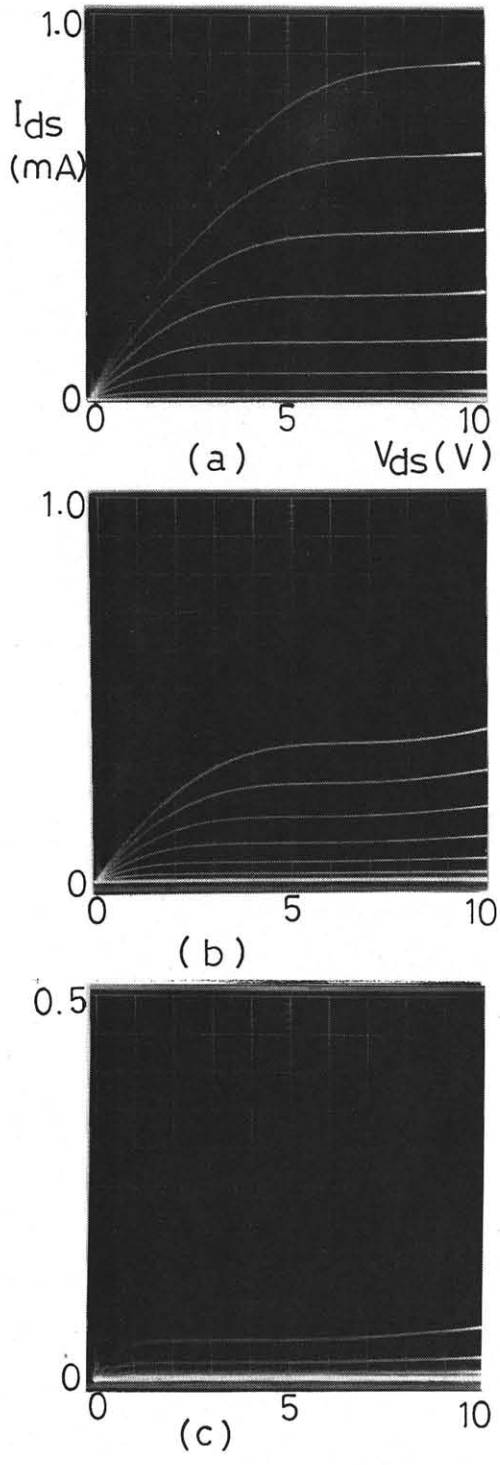

Fig.2 V_{DS} vs I_{DS}characteristics
(a) twin gate (V_{G1} and V_{G2})
(b) top gate (only V_{G1})
(c) bottom gate (only V_{G2})
V_{G1} : 0 to 5 V (0.5 Vstep)
V_{G2} : 0 to 25V (2.5 Vstep)

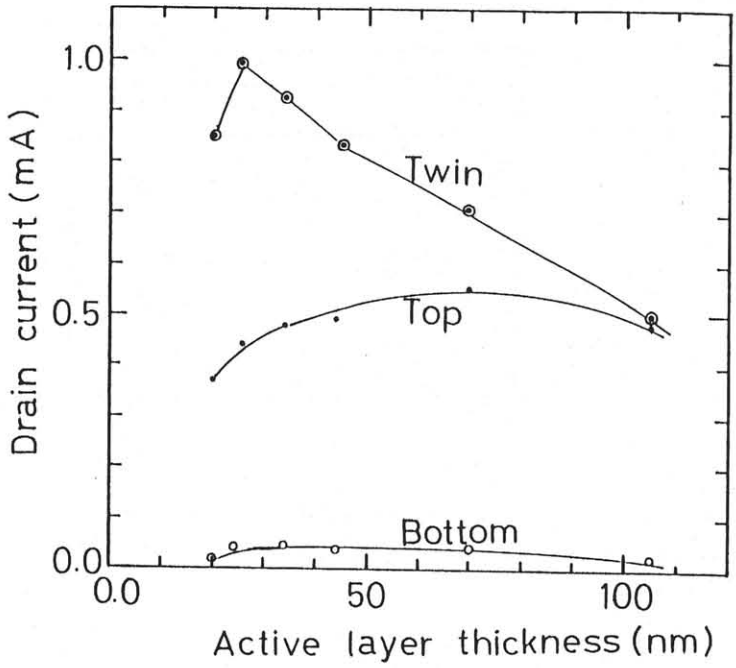

Fig.3 Thickness dependence of drain current as a parameter of gate bias condition(V_{DS} = 10V)

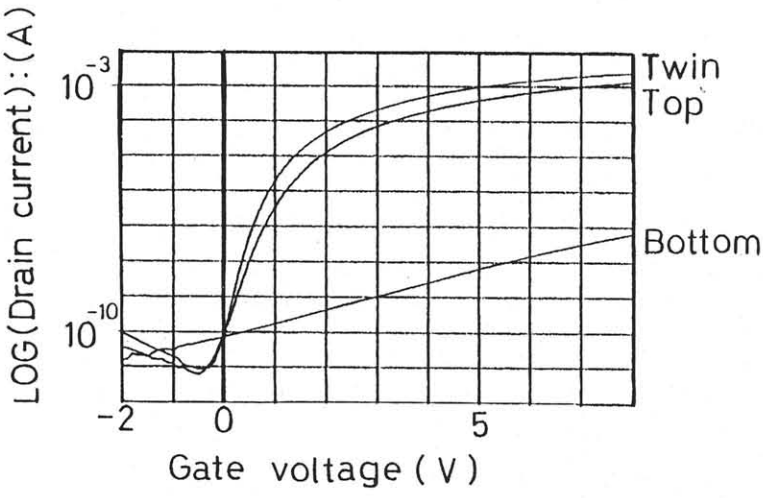

Fig.4 LOG(drain current) vs gate voltage with gate bias condition as a parameter(V_{DS} = 10V)

Table.1 Electrical characteristics

		twin gates	top gate	bottom gate
g_m	uS	235	110	8
I_{DS}	uA	990	420	40
S	mV/dec.	142	250	2300
V_{th}	V	0.8	1.2	20.0
C_g*	fF/um^2	0.74	0.67	0.067

*calculated

capacitance. Moreover, the bottom gate bias can be reduced by thinning the gate insulator film.

4. Summary

A superthin film transistor with twin gates was fabricated and measured. The large increase of the drain current was observed and the threshold voltage and sub-threshold slope were reduced by the twin gates structure. The thickness dependence of the effects was first observed and the optimum thickness was found to be 20-70nm thick. The ratio of the top and the bottom gate insulators must be designed at optimum condition. These devices have been applied to the silicon tramsistors with high speed operation as well as polysilicon thin film transistors. Especially, it is a key point to note the short channel effects can be suppressed while the transconductance is increased.

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