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A New Thermostable Ohmic Contact to n-GaAs —n^+-Si/n-GaAs Structure—

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n^+-Si has been found to be ohmic contacts to n-GaAs. The n^+-Si films were formed on n-GaAs by conventional vacuum evaporation and P^+ ion implantation. Even after annealing at 850°C, the surface and the interface of the n^+-Si/n-GaAs structure were uniform and ohmic contact characteristics were observed. By using Al as electrodes on the n^+-Si film, the contact resistivity of about 1.5 Ω·mm was obtained, which was only three times higher than that of the conventional Au-Ge alloyed contact. MESFETs were fabricated and the Al/n^+-Si contact to n-GaAs was found to be stable at least up to 500°C.

1. Introduction

For fabrication of GaAs integrated circuits(ICs), thermally stable ohmic contacts are highly desirable in order to deposit passivation films, to use Al as interconnects, and to construct multilevel interconnections. Moreover if the contacts are stable at temperatures required to activate ion implanted species, then new device fabrication processes using self-aligned techniques will become possible.

Alloyed metals such as Au-Ge based alloys has been widely used for the ohmic contacts to n-GaAs. However, such alloyed contacts have problems from the view point of thermal stability.[1] For instance, they tend to have an irregular surface morphology and an instability in contact resistance after a heat treatment at temperatures above 400°C. As a non-alloyed contact to n-GaAs, n^+-Ge has been found to show good ohmic characteristics.[2,3] But the n^+-Ge contact does not satisfy the above requirements because diffused Ge into GaAs detrimentally affects the ohmic characteristics.[3]

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In this work, we propose n^+-Si as a new ohmic contact material, and demonstrate that n^+-Si/n-GaAs structure prepared by conventional vacuum evaporation and ion implantation techniques shows a good ohmic characteristic and a very smooth surface even after annealing at 850°C.

2. Experiments

The n^+-Si/n-GaAs contacts were electrically characterized by the transmission line method (TLM). Figure 1 shows the typical preparation procedure of the samples for the TLM. GaAs used in this work was epitaxial wafers consisting of an n-layer having carrier concentration of $1x10^{17}cm^{-3}$ on semi-insulating(S.I.) GaAs. The wafer was chemically cleaned and loaded into a vacuum chamber having a background pressure less than $5x10^{-6}$Pa. Si of 10N purity was evaporated onto the GaAs substrate at room temperature. No attempt was made additionally to clean the substrate surface before the deposition. The deposition rate of Si films was about 5nm/min and the thickness was about 200nm. After the deposition of Si films, the samples were annealed at 400°C for 1 hour in the vacuum chamber in order to densify the Si film. P^+ ions were implanted into the samples. The dose of P^+ ions was $5x10^{15}cm^{-2}$ and the energy was 90keV. At this energy, the maximum in depth profile of the P concentration is positioned near the center of the Si film. After the implantation, the samples were annealed at 850°C for 15 min in N_2 atmosphere without encapsulation films on the sample surface. Then, in order to make the TLM patterns, Al patterned by a lift-off process was used as the mask for the etching of the Si film by using CF_4 plasma. Finally the Al electrodes were sintered with the Si film at 350°C for 10min.

Besides the TLM, the Si films were characterized by transmission electron microscopy(TEM) and the four point probe method. MESFETs were also fabricated in order to examine feasibility of the n^+-Si contacts for device application.

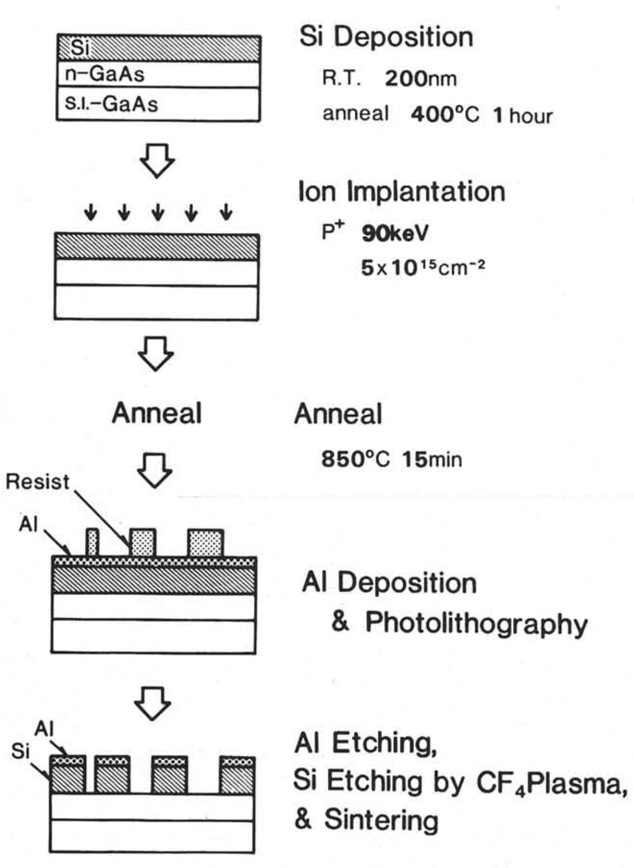

Fig. 1. Preparation procedure of Al/n^+-Si TLM patterns on an epitaxial n-GaAs wafer.

3. Results and Discussions

3.1 Properties of Si films

Figure 2 shows a cross-sectional TEM micrograph of the n^+-Si/GaAs structure after P^+ implantation and annealing at 850 °C. We can see the very smooth surface and interface. No alloyed layer is observable at the interface. The Si film is found to be polycrystalline. The grain size of the Si film was about 1μm on the average. This size was almost similar to the grain size of Si films formed by the same procedure on SiO_2/Si structures. These results indicate that the crystalline information does not transfer from the GaAs substrate to the Si film as far as the above mentioned process is employed.

The sheet resistivity of the n^+-Si films on GaAs was about 30Ω/□. This value was identical to that of a Si film formed on a SiO_2/Si structure.

3.2 Ohmic contact characteristics

By using the Si film implanted to the dose of $5x10^{15}/cm^2$ and annealed at 850°C for 15min, ohmic contacts have been obtained as shown in Fig. 3. The current-voltage(I-V) characteristic in this figure was taken between two adjacent electrodes in the TLM

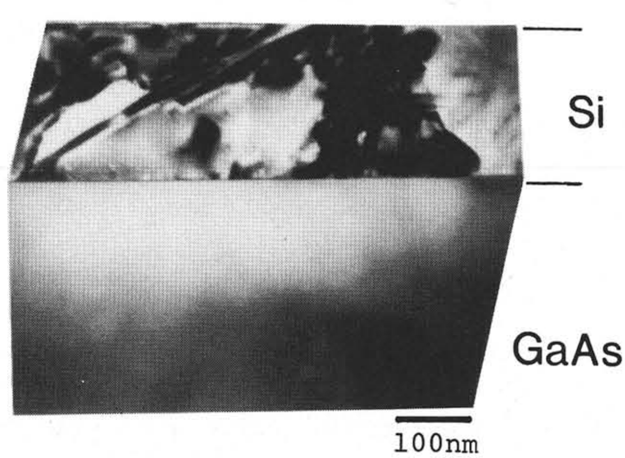

Fig. 2. Bright field cross-sectional TEM micrograph of a Si/GaAs(100) structure. The sample was annealed at 850°C for 15 min after P^+ ion implantation.

pattern. Figure 4 shows a typical resistance vs. gap of electrode(R-l) characteristic obtained from the TLM. The specific contact resistivity r_c of the Al/n^+-Si/n-GaAs system obtained from this characteristic is about $3.4\times10^{-4}\ \Omega\cdot cm^2$. The r_c between Al and n^+-Si has been found to be about $3\times10^{-5}\Omega\cdot cm^2$. Thus the above r_c value indicates the contact resistance between n^+-Si and n-GaAs. This r_c value is more than one order higher than r_c values obtained from usual Au-Ge alloyed contacts. But the specific contact resisitvity r_c calculated from the TLM results is not suitable for comparison between alloyed and non-alloyed contact, because the usual TLM assumes that the resistivity of the conductive layer beneath the contacts is unaltered even after alloying. Thus we define the contact resistivity ρ_c normalized by the width of the contact electrodes. Further the ρ_c is more suitable indication of the contact resistance for such devices as MESFETs. Table 1 shows the comparison of the ρ_c between the present Al/n^+-Si non-alloyed contacts and Au-Ge alloyed contacts formed on the same GaAs wafers. The ρ_c of the Al/n^+-Si/n-GaAs system is only three times higher than that of the Au-Ge/n-GaAs system.

It is noteworthy that the sheet resistivity of the GaAs active layer estimated from the gradient of the plot in Fig. 5, which is about 64Ω/□, is lower than that of the starting material(about 300Ω/□). This suggests that diffusion at the interface takes place during annealing at 850°C.[4]

3.3 MESFET fabrication

Figure 5(a) shows schematic cross-section of a MESFET fabricated by using the n^+-Si contact for the source and drain. The GaAs used was an epitaxial n($n=1\times10^{17}/cm^3$, 0.5μm thick) on S. I. wafer. The n^+-Si contacts were patterned by depositing a SiO_2

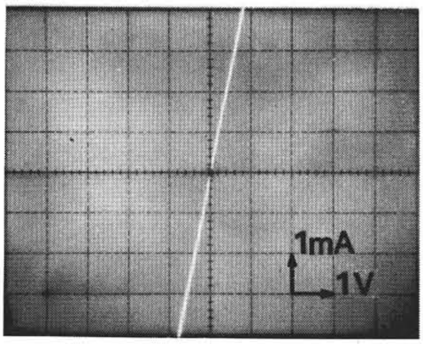

Fig. 3. I-V characteristic between two adjacent electrodes of the Al/n^+-Si TLM pattern on n-GaAs.

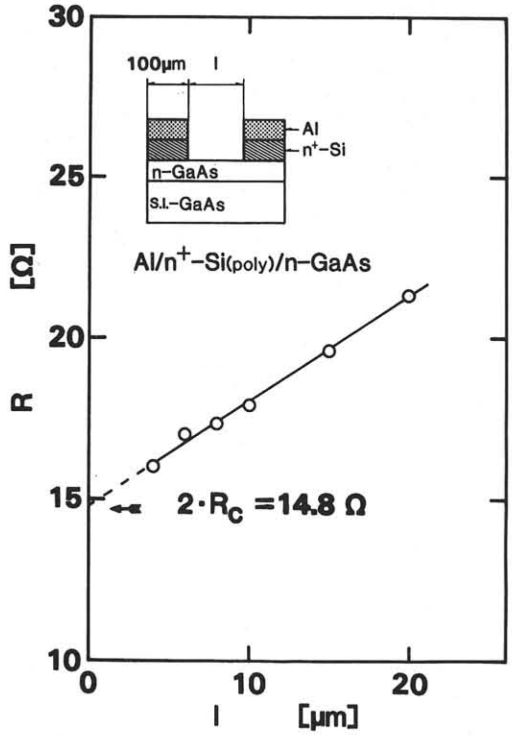

Fig. 4. Typical resistance vs. gap of electrodes (R-l) characteristic taken from the Al/n^+-Si TLM patttern on n-GaAs.

Table 1. Comparison of the specific contact resistivity r_c(normalized by the area) and the contact resistivity ρ_c(normalized by the width) between n^+-Si and Au-Ge contacts formed on the same GaAs wafer($n=1\times10^{17}/cm^3$).

	r_C [Ω·cm²]	ρ_C [Ω·mm]
Al/n^+-Si	3.4×10^{-4}	1.48
Au-Ge	1.0×10^{-5}	0.50

n-GaAs $1\times10^{17}\ cm^{-3}$

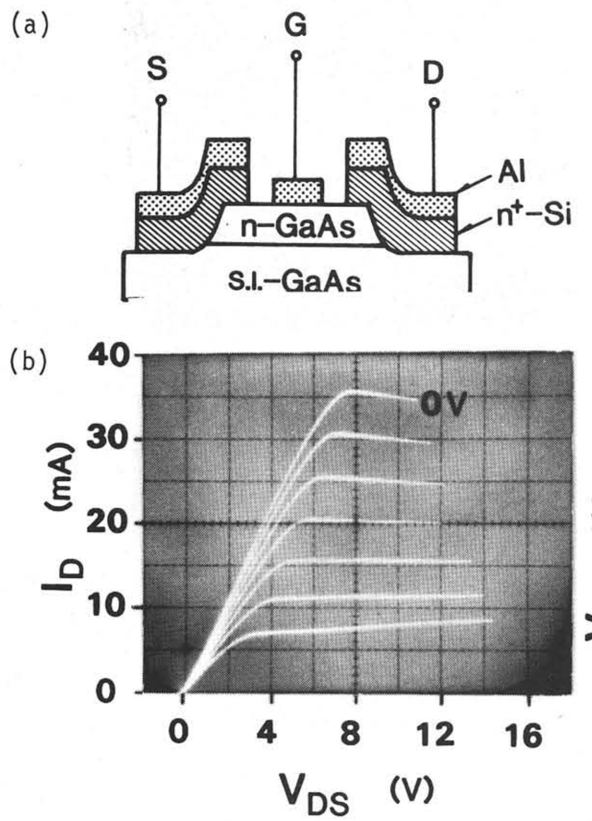

Fig. 5. (a)Schematic cross-section of a MESFET fabricated by using the n^+-Si ohmic contacts as the source and gate electrodes. (b)Typical I_d-V_d characteristic of a MESFET having the gate length of 7 μm and the gate width of 140 μm.

film having windows at the source and drain regions. After P^+ implantation and annealing at 850°C, the Si and SiO_2 films at the gate region was removed by CF_4 plasma etching using Al on the source and drain n^+-Si contacts as the mask. Al was used as the gate electrode, which was patterned by the lift-off technique.

Figure 5(b) shows a typical drain current vs. drain voltage(I_d-V_d) characteristic of a MESFET having a gate length of 7 μm and a gate width of 140 μm. The trans-conductance g_m calculated from this characteristic is about 36 mS/mm.

In order to check the thermal stability of the Al/n^+-Si ohmic contact, the MESFETs were annealed at 500°C for 10min in N_2 atmosphere. The drain characteristic after the annealing was the same as that before the annealing. These results demonstrate that the n^+-Si ohmic contact is feasible for device application and tolerant for various kind of processing technologies.

4. Conclusion

n^+-Si can be used as non-alloyed ohmic contacts to n-GaAs, which is stable at temperatures required to activate implanted species. The n^+-Si ohmic contact can be formed only by conventional vacuum evaporation and ion implantation techniques. By using the n^+-Si contact, Al can be used as interconnect material. The Al/n^+-Si/n-GaAs contact is stable at least up to 500°C.

The above characteristics can remove the problems of the use of the conventional Au-Ge alloys, though the contact resistance of the n^+-Si contact is higher at present than that of the Au-Ge alloy. Increase of the carrier concentration in both the Si layer and the GaAs layer will be effective to reduce the contact resistance.

Acknowledgments

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