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Analysis of Planar Channeling Effects on the Threshold Voltage Uniformity of GaAs MESFETs Using Stereographic Projection

Hitoshi MIKAMI, Naotaka UCHITOMI, and Nobuyuki TOYODA

VLSI Research Center, Toshiba Corporation

1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki, 210, JAPAN

Planar channeling effects on 3-inch GaAs wafers with a (001) surface were investigated to improve the threshold voltage uniformity of GaAs MESFETs over an entire wafer using a stereographic projection technique. This technique was found to be very useful for a quantitative understanding of the relationship between the direction of an incident ion beam and the wafer orientation during implantation. The ratio, $N(X_1)/N(X_2)$, of peak carrier concentration at a depth of X_1 to carrier concentration at depth of $X_2=2X_1$, obtained from the carrier depth profiles, was mapped over an entire wafer to determine the area where the planar channeling occurred on a stereographic projection. The most uniform implants were obtained at an azimuthal angle of 26.5° by tilting the wafer 10°, as a result of analytical and experimental procedures.

I. Introduction

In recent years, the planar channeling effects have become a crucial problem in controlling the threshold voltage (V_{th}) with fine accuracy for realizing LSI-grade GaAs ICs. Kasahara, et al., reported on the effect of channeling on V_{th} distribution in a 2-inch GaAs wafer[1]. They showed an improvement of V_{th} uniformity by changing the tilt angle from 6° to 10°, and also obtained uniform V_{th} distribution throughout the 2-inch wafer using a tilt angle of 9° and an azimuthal angle of 22.5°. However, a systematic investigation for obtaining optimized angular conditions, especially azimuthal angular conditions, to prevent planar channeling effects is required to realize more uniform implants.

In this paper, we describe an analytical technique for understanding the channeling effects using stereographic projection, and propose an azimuthal angle for minimizing the planar channeling effects, as a result of both analytical and experimental procedures.

II. Analytical procedure

The key issue in controlling planar channeling effects is the understanding of the angular relationship between the incident beam direction and the direction of the major crystal plane. Figures 1(a) and (b) illustrate the wafer orientation parameters and the angular parameters for an electrostatic-scan implantation system used in this paper, respectively. A wafer having a (001) surface and a (110) reference flat is assumed in this figure. The ion beam deflection angles for horizontal(X) and vertical(Y) scanning across center-to-edge in a 3-inch wafer are depicted as Δ_x and Δ_y, which were calculated to be 1.55° and 1.36°, respectively, from the geometry of the used implantation system. Figure 2 shows the angular relationship between the incident beam direction and the wafer orientation angles on a part of a stereographic projection of a cubic crystal (usually called Wurff net). The drawn stereographic projections, ranging from 0° to 10°, can be given by usual polar coordinates without serious error. In this figure, the radial direction(θ) from the center, which means the (001) major crystal plane, and the azimuthal angle(ϕ) from the [110] direction correspond to the tilt and azumuthal angles of an implanting wafer mounted on a holder, respectively. Thus, an accurate relationship between the wafer orientation with the (001) surface and the incident beam upon the point "a" in the wafer indicated in Fig.2 inclines its direction toward the [110] direction by angle Δ_x compared with the wafer center. In addition, this method is applicable to Si wafers as well as GaAs wafers.

III. Experimental procedure

Silicon ions were implanted at 150keV with a 3.5×10^{12} cm^{-2} dose into 3-inch undoped semi-insulating GaAs substrates with a (001) surface and a (110) reference flat. To ensure precise wafer orientation, a specially designed wafer platen was attached to the implantation system. GaAs wafers were tilted to 7° and 10°, varying the azimuthal angles from 0° to 90° away from the [110] direction in the tilted plane.

After implantation, the wafers were annealed at 820°C for 20 minutes in an AsH_3+Ar atomsphere. Ti/Pt/Au was evaporated and delineated by the conventional lift-off technique to define 1mm diamater Schottky diode patterns over the entire wafer.

Carrier concentration profiles were measured using the automated capacitance-voltage (C-V) method. The carrier depth profiles are shown in Fig.3. As the wafer was tilted to 7° with an azimuthal angle of 0°, planar channeling effects of a set of {110} planes appeared in the carrier profiles.

In order to investigate the planar channeling effects in the present experiments, the ratio R of $N(X_1)$ to $N(X_2)$ was employed as a suitable parameter which effectively reflects the variation in the carrier profiles arising from the planar channeling effects. Then, the carrier concentration $N(X_1)$ and $N(X_2)$ at depths of X_1 and X_2 from the surface were picked up from the carrier concentration profiles, in which X_1 corresponds to the depth of the

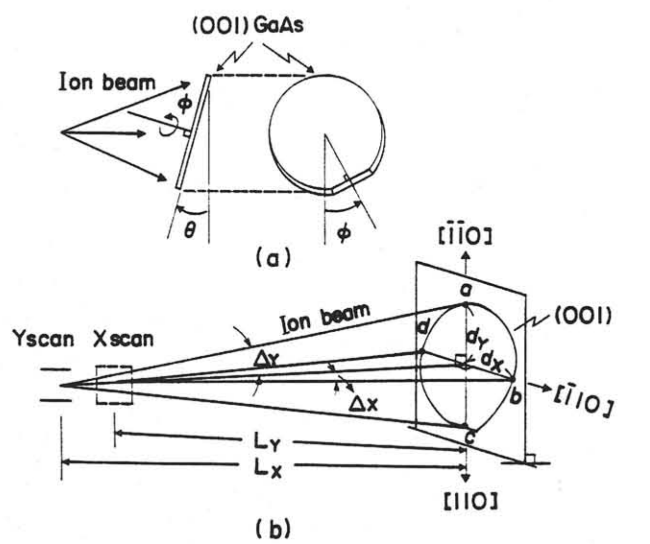

Fig.1 (a) Wafer orientation parameters: θ and ϕ mean tilt and azimuthal angle during implantation. (b) Angular parameters for electrostatic-scan implantation system used in present experiment.

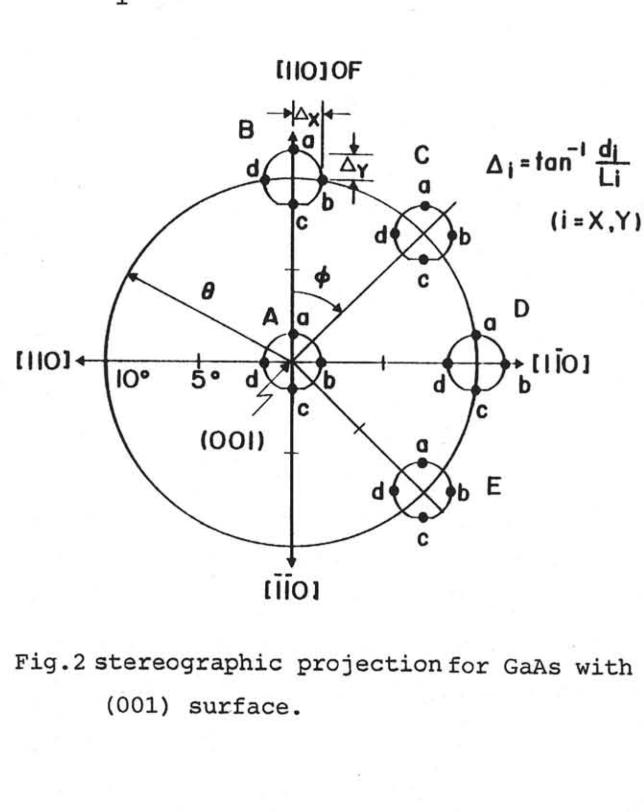

Fig.2 stereographic projection for GaAs with (001) surface.

peak carrier concentration and X_2 was chosen as $2X_1$, as indicated in Fig.3. The ratio of $N(X_1)$ to $N(X_2)$ was calculated and mapped over the whole wafer. If the implanted proflies are assumed to be Gaussian, the parameter R is expressed as

$$R=N(X_1)/N(X_2)=\exp(Rp/\Delta Rp)^2 \qquad (1)$$

where Rp and ΔRp are the projected range and range straggle, respectively. As Rp corresponds approximately to the location of X_1, the measured R can be represented as $R=\exp(X_1/\Delta Rp)^2$. Thus, this parameter can remove additional effects, such as dose fluctuation during implantation.

The pinch-off voltage, Vp, was also derived from the product of carrier concentration, N(X), and depth, X.

IV. Results and Discussion

Figure 4 shows the variation in R and Vp as a function of the azimuthal angle(ϕ) ranging from 0° to 45° for tilted wafers at 7°. Minimum values of R appeared at 0° and 45°, corresponding to the results from {110} and {100} planar channeling was found to be much larger than that of {100} planar channleing by comparing the R-values. On the other hand, a maximum value of R was indicated at an azimuthal angle of 30°. The calculated threshold voltages were dependent very little on the azimuthal angles ranging from 20° to 35°, in which R showed values larger than 6. Thus, the azimuthal angle of 30° can be concluded to be optimal for minimizing the plannar channeling effects in a GaAs wafer with a (001) surface. However, as will be shown in Fig.5, this angular condition for reducing planar channelings is valid only near the center section of a 3-inch wafer and for an implanter system with a flex beam angle varying from 0° at the center to 0.4° at the 3-inch wafer edge.

Figure 5 represents an R-map on a stereographic projection. The dotted field corresponds to that for R values smaller than 6, which is considered in this experiment as the extent to which planar channeling affects threshold voltage uniformity by referring to the result of Fig.4. As evident from Fig.5, the result reveals that, as long as this type of implantation system is used, planar channeling in a 3-inch GaAs wafer cannot be prevented by tilting the wafer to 7°. On the other hand, it is predicted from this figure that more uniform implants can be obtained by varying the tilt angle from 7° to 10°. Since the azimuthal angles showing

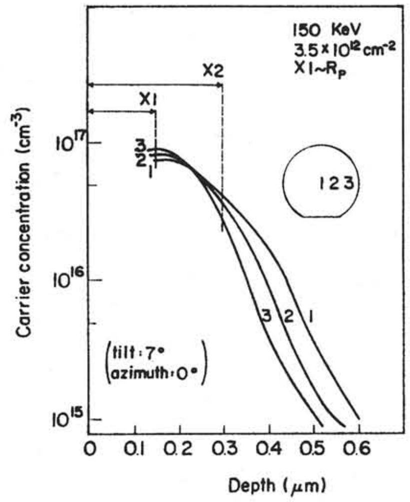

Fig.3 Carrier depth profiles

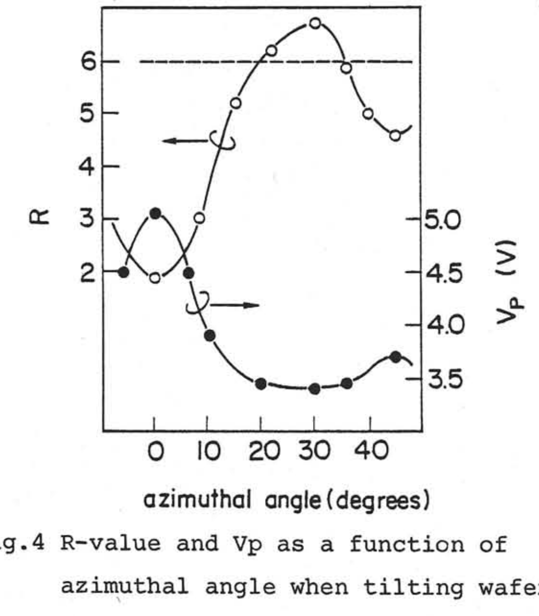

Fig.4 R-value and Vp as a function of azimuthal angle when tilting wafer 7°.

R≧6 is evaluated to range between 16° and 37° at a tilt angle of 10° on the basis of the experimental results obtained at a tilt angle of 7°, it is concluded that the aziumthal angle for minimizing planar channeling effects is 26.5° in the 10° tilting plane.

Figures 6(a) and (b) illustrate the distribution maps for the R-values of wafers implanted at (a) $\theta=7°$ and $\phi=30°$ and (b) $\theta=10°$ and $\phi=26.5°$, in order to confirm the prediction mentioned above. The angular conditions are indicated on the stereographic projection in Fig.5. Fourty-nine percent of the measured area of a wafer implanted under the (a) angular condition showed R-values larger than 6. On the other hand, the area indicated by R larger than 6 was enlarged up to 91 percent in a wafer implanted under the (b) angular condition. As an important result, the effects of the {100} and {110} planar channelings were clearly improved by a tilt angle of 10° rather than 7°, and the most uniform implants were obtained by an azimuthal angle of 26.5°.

V. Conclusion

In the present study, we demonstrated that the stereographic projection technique is very useful for understanding the angular relationship between the incident beam direction and the orientation of the major crystal planes during implantation. As a result of both analytical and experimental investigations, the azimuthal angle for minimizing the planar channeling effects in GaAs was found to be 26.5° when tilting the wafer at 10°.

Acknowledgments

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References

1) J. Kasahara,et al., Tech. Digest GaAs IC Symposium, 1985, 37

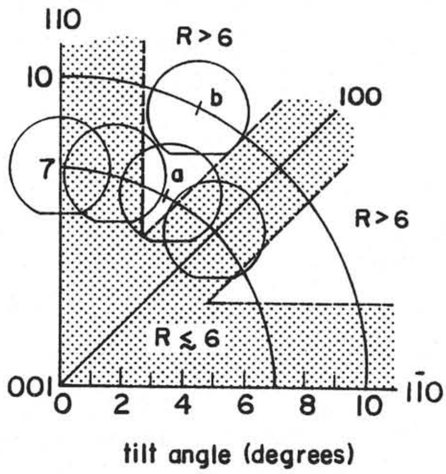
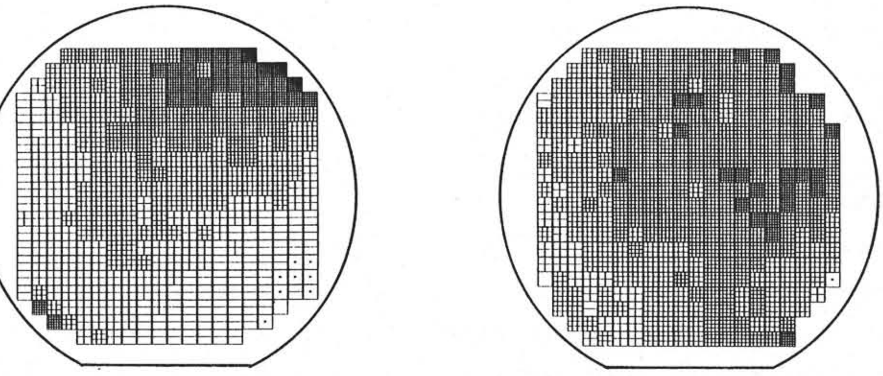


Fig.5 R-map on stereographic projection.



(a) (b)

⊡: 4.5 ≦R ≦5.0 ⊟: 5.0 ≦R ≦5.5 ⊞: 5.5 ≦R ≦6.0 ▦: 6.0 ≦R ≦6.5
▦: 6.5 ≦R ≦7.0 ▦: 7.0 ≦R ≦7.5 ■: 7.5 ≦R ≦8.0

Fig.6 Distribution maps for R-values of wafers implanted at (a) $\theta=7°$ and $\phi=30°$ and (b) $\theta=10°$ and $\phi=26.5°$.