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A Model of the Surface State Distribution for AlN/GaAs System

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Electrical properties of metal-insulator-semiconductor (MIS) of AlN/GaAs structure were investigated by capacitance-voltage (C-V) and isothermal capacitance transient spectroscopy (ICTS). An energetically discrete level (E_C-0.65eV) near the interface was detected both by the ICTS and analysis of C-V characteristics by the Terman method. From the simultaneous measurements of n-GaAs and p-GaAs MIS structure, there exits another discrete level of huge density (E_C-0.9eV) at the interface. A model of interface state distribution for AlN/GaAs system is presented.

1. Introduction

The understanding and control of the electrical and structural characteristics of the III-V semiconductor surface and interface are of great importance both technologically and physically. Presently Fermi level at the surface or interface (E_{fs}) is pinned during metal and/or insulator deposition regardless of what foreign atoms are deposited, whereas, on the contrary, very low surface-state density (N_{ss}) results at the lattice-matched semiconductor heterojunction. The mechanism of pinning, therefore, has been a controversial subject and several models have been reported[1-4]. None of the models, however, can be necessarily applicable to all the real interfaces: some are good only for metal-semiconductor (M-S) interface, and others are good for heterojunction or insulator-semiconductor (I-S) interface.

For the case of I-S interface, it is difficult to construct a rationalized pinning model since well-defined electrical and structural experiments are lacking. The reason is partially because, in the present III-V M-I-S system, there is always a strong pinning of E_{fs} which made it difficult to reveal the true face of the interface by an electrical method[5]. There is also a problem of the residual native oxides of the host semiconductor between I-S interface, which is known to have the complex phases[6], bringing some problem of reproducibility of fabricating M-I-S structure.

Recently we have reported the successful low-temperature deposition of AlN on n-GaAs and n-InP to make M-I-S structure[7], for which the drastic reduction of N_{ss} near the conduction band was achieved[8]. The result is quite reproducible and we think that this is enabled by a successive growth of GaAs and AlN in the same growth chamber by MOCVD to exclude the formation of the complex native oxides. In this paper we extend our study to p-GaAs M-I-S structure to evaluate electrical characteristics of the generalized AlN/GaAs I-S interface. Following sections include extended experimental data supporting our previous study for n-GaAs M-I-S system[8], characteristics of AlN/p-GaAs interface and conclusion of our model of interface state distribution.

2. Experimental

Details of the growth procedures of AlN on GaAs are reported elsewhere[7]. It is noted here that lower N_{ss} was obtained when growing n- or p-GaAs epitaxial layers (typically at 650°C) followed by an AlN deposition (thickness of 700Å, typically at 370°C) in the same reactor. For the characterization purpose, some diodes are made on bulk-GaAs with AsH_3 pre-treatment for which N_{ss} is somewhat higher than an epitaxial GaAs case[8].

A MIS diode was fabricated by evaporating Au or Al and soldering Indium for a back ohmic contact. C-V characteristics shown in this paper were taken with a voltage sweep rate of 0.5V/sec from negative to positive gate voltage (V_G).

3. Results and Interpretation

a) AlN/n-GaAs system

A typical C-V characteristics of Au/AlN/n-GaAs system is shown in Fig. 1 for frequency range between DC to 5 MHz. The frequency dispersion of the capacitance for this diode is thought to be quite small if considering some of the dispersion at the accumulation side is coming from AlN insulating film itself as shown in the inset for the Al/AlN/n^+-GaAs structure.

In the previous paper we have shown that the peak 1 (E_C-0.65eV) observed in the N_{ss} vs. energy profile (Fig. 2) is a semi-discrete defect level by comparing it with Isothermal Capacitance Transient Spectroscopy (ICTS). To prove this further we measure the ICTS intensity with an appropriate bias, pulsing and temperature conditions. In order to pick up the signal from peak 1, following measurement conditions are used: temperature T=297K, electron injection by pulsing the gate voltage to V_G=18V with a duration of 5msec. Obtained ICTS peak-intensity was divided by the junction capacitance to correlate the defect concentration and the results are plotted in the left half of Fig. 3 as a function of the fixed gate bias. It is clear that the shape of bias dependence of the ICTS signal and the peak 1 in the N_{ss} vs. bias plot (the right half of Fig. 3 which is converted from Fig. 2) are quite similar, indicating that the same level involved in two different methods. For the next step, we measured temperature dependence of the emission time constant of the peak 1 at two fixed bias conditions (3V and 6V which correspond to both side of the peak), expecting two different activation energies since the peak1

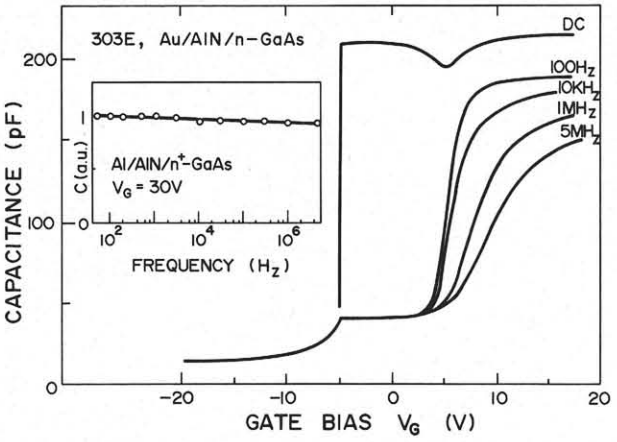

Fig. 1 C-V characteristics of Au/AlN/n-GaAs(epitaxial layer) structure. The inset shows dependence of C on frequency for Al/AlN/n^+-GaAs at V_G=30V.

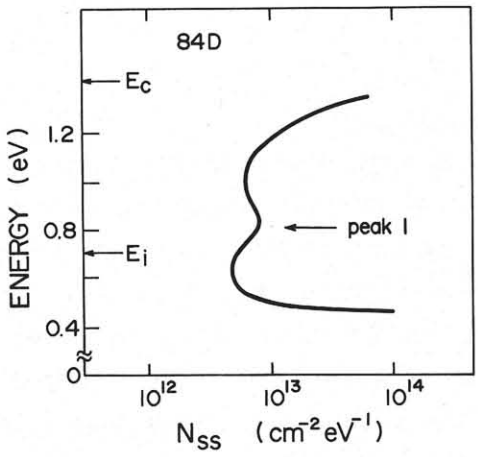

Fig. 2 Nss distribution for a MIS diode calculated from 1MHz C-V characteristics. Note that bulk GaAs was used as a semiconductor.

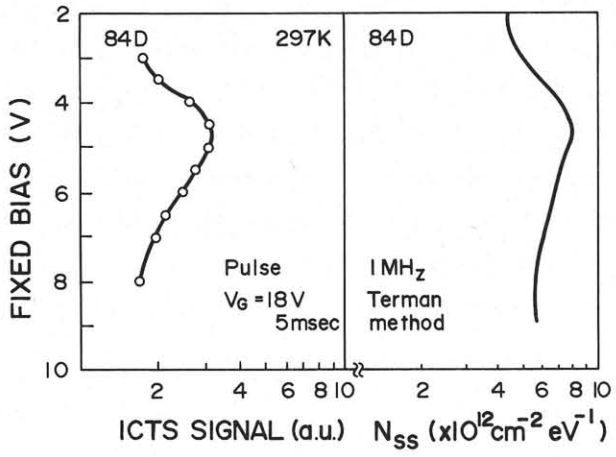

Fig. 3 ICTS intensity of peak 1 as a function of gate bias (left). Nss distribution vs gate bias for the same sample (right).

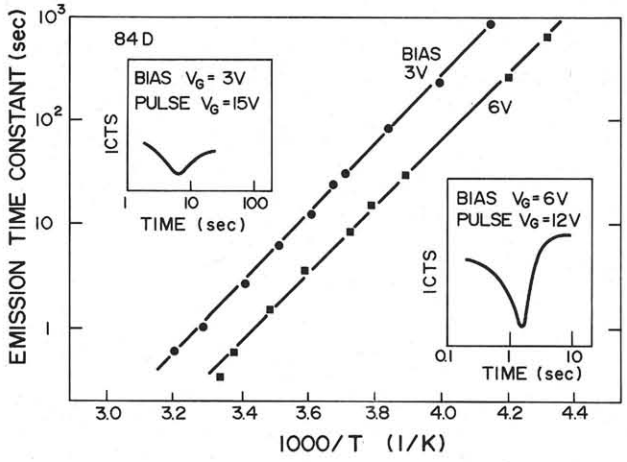

Fig. 4 Temperature dependence of emission time constant for peak 1. Circles are taken at V_G=3V, squares at V_G=6V.

seems to have some energy distribution. Arrhenius plots are shown in Fig.4, however, showing the exactly same value for two conditions (E_c-E_t=0.644eV, note for a quite similar value for the peak 1 in Fig. 2). This fact suggests that the level 1 (corresponding to peak 1) is an energetically discrete level rather than a continuous or semi-discrete (bound of a number of discrete levels) one. Furthermore, since E_{fs} is different for 3V and 6V bias and yet the same discrete level is detected, the level 1 should exist extending into the semiconductor. It is noted here that electron emission properties of this level (see insets of Fig. 4) suggests larger cross section for 6V bias. Since, for 6V bias, the level at the interface is mainly involved cross section of the level at the interface seems to be larger than that in the semiconductor.

The results and discussion here have shown the N_{ss} profile deduced by the Terman method is correct in terms of energy scale since the energy is calibrated by determining the energy depth of the peak 1 independently from the Arrhenius plot of the ICTS signal.

b)AlN/p-GaAs system

An AlN/p-GaAs structure was fabricated for which p-GaAs was epitaxially grown on p^+-GaAs substrate. C-V characteristics of this diode is shown in the inset of Fig. 5; the behavior is quite symmetrical to that of the n-GaAs M-I-S diode for the gate bias. It is especially noted that there is a deep depletion at the depletion-inversion side, very similar to n-GaAs case. This deep depletion in p-GaAs as well as in n-GaAs disappears when a sample is irradiated by a sub-bandgap light. Therefore we speculated that the deep-depletion is due to the strong pinning to an interface state of huge density. The N_{ss} profile of AlN/p-GaAs system is calculated[9] by the Terman method and shown in Fig. 5 together with AlN/n-GaAs system of Fig. 2. There is a remarkable fit of the steep increase of N_{ss} at E_c-0.9eV for both n- and p-GaAs M-I-S system, strongly indicating that the deep depletion results because of pinning to a defect of huge density. Also the type of this defect looks discrete from its narrow energy distribution.

4. Discussion

Here we propose a model of AlN/GaAs interface state distribution based on the experimental data shown above. First we observed a reduction of frequency dispersion of

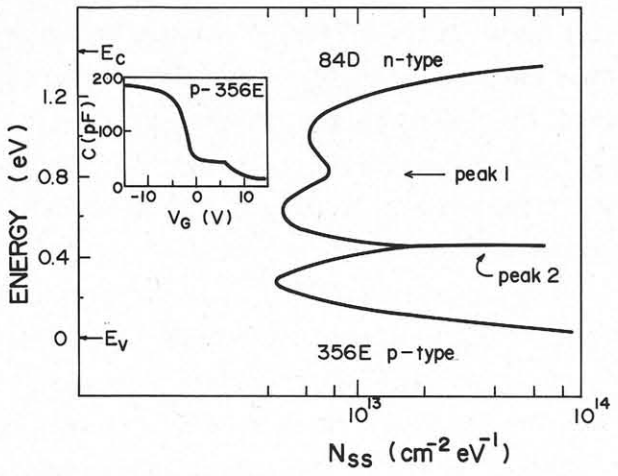

Fig. 5 Nss distribution for AlN/GaAs interface. The upper curve was determined for n-type MIS and the lower one was from p-type sample. The inset shows C-V characteristics for Au/AlN/p-GaAs structure at 1MHz.

the capacitance which corresponds to the decrease of N_{SS} near the conduction band. In our previous paper, decrease in level 1 concentration and that in the continuous surface state near the conduction band resulted simultaneously[8]. However we observed here that the characteristic electron emission response of the level 1 is much smaller than the frequency range of 100KHz to 5MHz where the frequency dispersion is typically notable. In this context the observed decrease in frequency dispersion is due to the reduction of continuous surface states. It is apparent, therefore, that interface states consist partly of U-shape continuous level. Secondary there is one distinct defect of which energy level is discrete, located at E_C-0.65eV. Thirdly there is a defect of huge density so that we could never sweep Efs over this level. However the existence of this defect and its discrete nature has been shown by the simultaneous analysis of p- and n-GaAs M-I-S structure. Therefore we conclude that AlN/GaAs interface consists of U-shape continuous level and two discrete levels. In the practical point of view, the way of reducing surface states is important and we found that the conduction band side of the U-shape surface states and the level 1 can be decreased in a proper As-treatment which will be reported elsewhere[10]. The concentration of the level 2, however, remain unchanged in the course of our present experiment. Because of its high density, we think that this is the level which strongly pins the surface potential in the I-S interface and could be in the M-S interface.

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9)There is some ambiguity determining the carrier concentration of p-GaAs since the values evaluated by three different approaches are not the same: 6-7X10^{14} cm^{-3} by the Hall measurement for a layer grown on SI substrate in the same run, 1X10^{16} cm^{-3} by the C-V measurement of the Schottky diode made from the same chip by removing AlN film by phosphoric acid and 3X10^{15} cm^{-3} by C-V analysis of the deep depletion characteristics of M-I-S structure. We take the value 3X10^{15} cm^{-3} for the calculation for Fig. 5 but the main conclusion discussed later remain unchanged even if any of three values is adopted in the calculation.

10)S.Fujieda and M.Mizuta unpublished.