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Growth of GaAs Layers on (001) Si Substrates

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GaAs layers with smooth, specular surfaces without scale-like steps were grown on (001) just Si substrates by MOCVD, using a thermal cycle treatment of the buffer layer. This treatment consists of a heating and a cooling of the buffer layer, and has large effects on the growth of GaAs on Si; it eliminates anti-phase defects, it interrupts the propagation of twins originating from the GaAs/Si interface and decreases the etch pit density from $5X10^8 cm^{-2}$ to $3X10^7 cm^{-2}$. Plane view SEM images of the buffer layer before and after the thermal cycle were observed and the effects of the buffer layer on the growth of GaAs overlayer were also studied.

1. INTRODUCTION

There is increasing interest in the heteroepitaxial growth of III-V compound semiconductors on Si substrates for electronic and optoelectronic applications[1-5] as well as for monolithic integration of Si and III-V devices.[6-8]

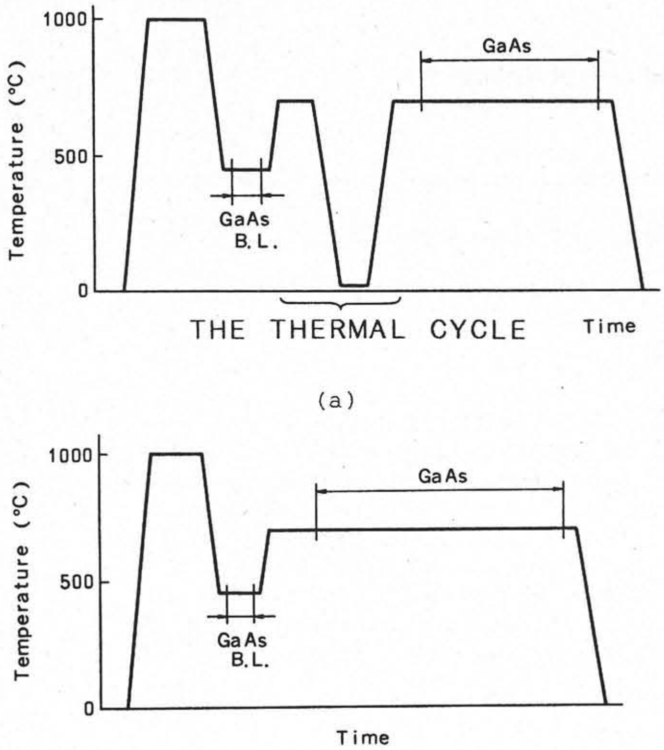
The growth of GaAs on Si has two serious problems, namely the large lattice mismatch of 4% and the growth of a polar semiconductor on a non-polar semiconductor. To overcome these difficulties, a thin GaAs buffer layer is grown at low temperature on a Si substrate, tilted towards <110> from (001); subsequent growth is done at the conventional growth temperature by MOCVD[9] or MBE.[10] Though the GaAs layers produced by such two-step growth have mirror-like surfaces,[9-10] the smoothness of these layers is not as good as that of homoepitaxially grown layers. Moreover, the use of tilted Si substrates brings scale-like surface morphology having undulations of 200-300A over 5μm. Such undulations would be a fatal problem for devices in which light or electrons are transported parallel to the substrate.

We have succeeded in growing GaAs layers with smooth, specular surfaces without scale-like steps on (001) just Si substrates by using a thermal cycle treatment of the buffer layer in a two-step growth sequence. This treatment consists of a heating and a cooling of the buffer layer. In this paper, the effect of this thermal cycle treatment are reported and it is compared with the ordinary two-step growth process.

2. EXPERIMENTAL

A low pressure MOCVD system was used for growth. Trimethylgallium (TMG) and arsine (AsH_3) were used as the source reactants with a carrier gas of H_2. The total flow rate and pressure were 5000 sccm and 130 Torr, respectively. Si (001) just wafers and Si (001) with 2° tilt toward <110> wafers were used as substrates. A Si wafer was placed on the pedestal in the reactor immediately after removing the surface oxide layer by dipping in HF. The substrate temperature was monitored by a thermocouple in the pedestal.

The GaAs layers were grown with the thermal cycle shown in Fig.1 (a). First, the Si substrate was heated to 1000°C for 30 min to remove any remaining surface oxide layer. Then, the substrate was cooled to the buffer layer growth temperature of 450°C. After growing a 100A GaAs buffer layer , the substrate was heated to 750°C and kept at that temperature for 10 min (first annealing). Next, after cooling to room temperature, the substrate was heated again to 750 °C and was again kept for 10 min (second



(b)

Fig.1 Temperature diagram of the thermal cycle growth (a) and the ordinary two-step growth (b).

annealing). Subsequently, the GaAs epitaxial layer was grown on the buffer layer under conventional growth conditions. For comparison, GaAs layers were also grown on Si substrates by the ordinary two-step growth technique illustrated in Fig.1 (b).

The surface morphologies of grown layers were examined by Nomarski microscope. The etch pit patterns of the layers etched by molten KOH were observed by scanning electron microscope (SEM). In order to investigate the effects of the thermal cycle on defects, cross-sectional transmission electron microscope (TEM) studies were performed.

3.RESULTS AND DISCUSSION

The Nomarski microphotographs of the grown layer surfaces are shown in Fig.2. The surface morphology of GaAs grown on (001) with 2° tilt toward <110> Si wafers with and without the thermal cycle are shown in Fig.2 (a) and (b), respectively. Both surface morphologies show scale-like steps with undulations of 200-300A (measured by Talystep). These steps are uniformly distributed over the GaAs surface and their size is almost independent of the thickness of the GaAs layers. The period of these scale-like steps decreased with the offset angle of the Si substrates. No remarkable difference of the surface morphology is seen between Fig.2 (a) and (b). Fig.2 (d) shows the surface morphology of GaAs grown on (001) just Si substrate without the thermal cycle. This has a very rough surface with pits and grooves. As shown later, this GaAs layer contains an anti-phase domain structure. On the other hand, the surface morphology of the GaAs layer grown on a (001) just Si substrate with the thermal cycle (Fig.2 (c)) is very smooth. This layer is free from anti-phase domains as shown below. The thermal cycling had large effects on the growth and eliminated the anti-phase domain, when (001) just Si was used for the substrates. The use of (001) just Si substrate also has the effects of reducing the scale-like steps.

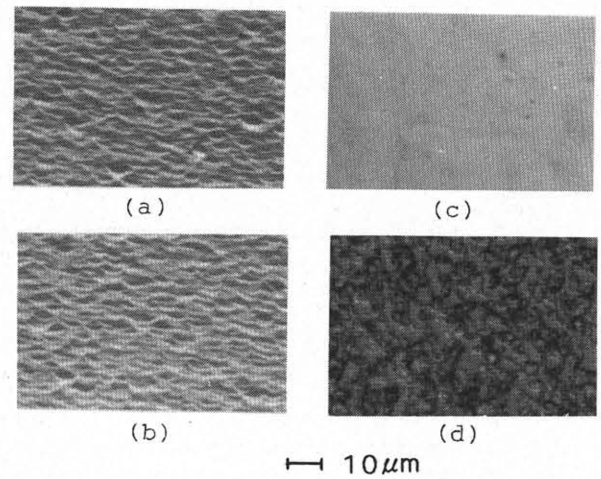
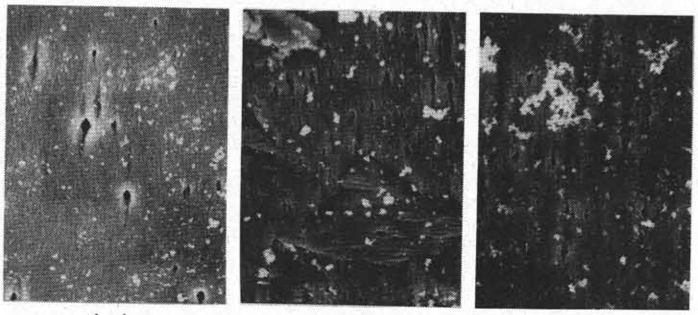


Fig.2 Nomarski microphotographs of the GaAs layer grown on (001) with 2° tilt toward <110> Si with the thermal cycle (a) and without the thermal cycle (b), and the GaAs layer grown on (001) just Si with the thermal cycle (c) and without the thermal cycle (d).

Figure 3 shows SEM microphotographs of the etch pit patterns of the samples etched by molten KOH. The etch pit pattern of the layer grown on (001) just Si without the thermal cycle (Fig.3 (b)) shows the existence of the anti-phase domain. The etch pit density (EPD) of this sample is about $5 \times 10^8 cm^{-2}$. On the other hand, the layer grown on (001) just Si substrate with the thermal cycle (Fig.3 (a)) is free from antiphase domains. This



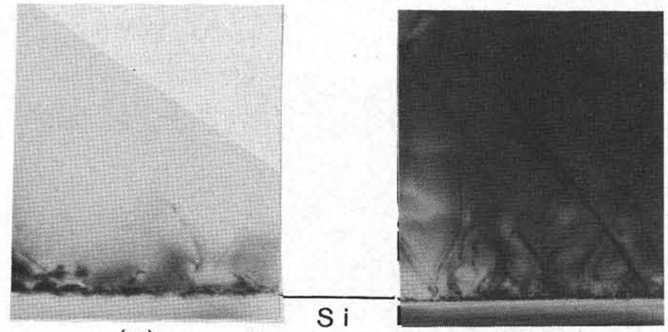
(a) (b) (c)

1 μm

Fig.3 SEM microphotographs of the etch pit pattern of the GaAs layer grown on (001) just Si with the thermal cycle (a) and without the thermal cycle (b), and the GaAs layer grown on (001) with 2° tilt toward <110> Si without the thermal cycle (c).

result indicates that the anti-phase domain structure can be eliminated by use of the thermal cycle (Fig.3 (a)). The EPD of this sample is about $3X10^7cm^{-2}$. This value is less than one tenth of that of the sample grown without the thermal cycle. The thermal cycle not only has the effect of eliminating anti-phase domains but also reduces the dislocation density. Fig.3 (c) shows the etch pit pattern of the GaAs layer grown on (001) with 2° tilted toward <110> Si substrate without the thermal cycle. The EPD of this sample is about $7X10^7cm^{-2}$. Comparison of this result with that of the sample grown on (001) just Si substrate using the thermal cycle (Fig.3 (a)) shows that growth with the thermal cycle and (001) just Si substrate are in no way inferior to the conventional two-step growth regarding dislocation densities.

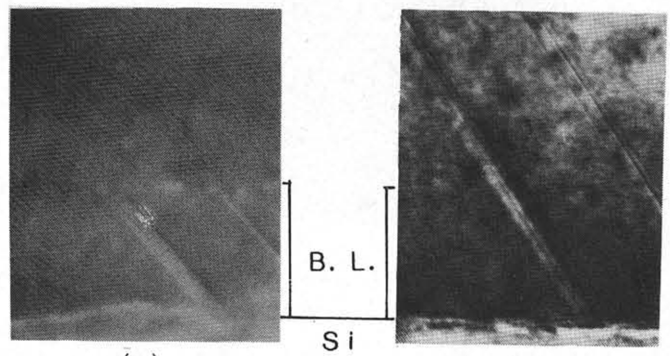
In order to examine the effect of the thermal cycle on the defect structure, TEM images were obtained from the layers grown on (001) just Si substrates with and without the thermal cycle. Fig.4 (b) shows the defect structures in the GaAs layer without the thermal cycle. There are many defects propagating out from the GaAs/Si interface into the epilayer. In addition to threading dislocations originating from the lattice mismatch, a number of plane defects running along a <111> direction were observed. In contrast to this, the TEM image obtained from the layer grown with the thermal cycle (Fig.4 (a)) shows that almost all the plane defects were eliminated. In



(a) (b)

200nm

Fig.4 Cross-sectional TEM images of the GaAs layers grown on (001) just Si with the thermal cycle (a) and without the thermal cycle (b).



(a) (b)

5 nm

Fig.5 Lattice images of the GaAs layers grown on (001) just Si with the thermal cycle (a) and without the thermal cycle (b).

addition, most threading dislocations had disappeared within 1μm from the GaAs/Si interface.

To investigate the elimination of the plane defects in detail, lattice images with high resolution transmission electron microscope (HRTEM) were observed. Fig.5 (b) shows the lattice image of GaAs grown on (001) just Si substrate without the thermal cycle. The plane defects which can be ascribed to twins from the results of the electron diffraction, originate from the GaAs/Si interface and run through the buffer layer to the GaAs epitaxial layer. On the other hand, the lattice image of the layer grown on (001) just Si substrate with the thermal cycle (Fig.5 (a)) shows that twins originate from the GaAs/Si interface, but stop at the interface between the buffer layer and the upper GaAs layer. This result

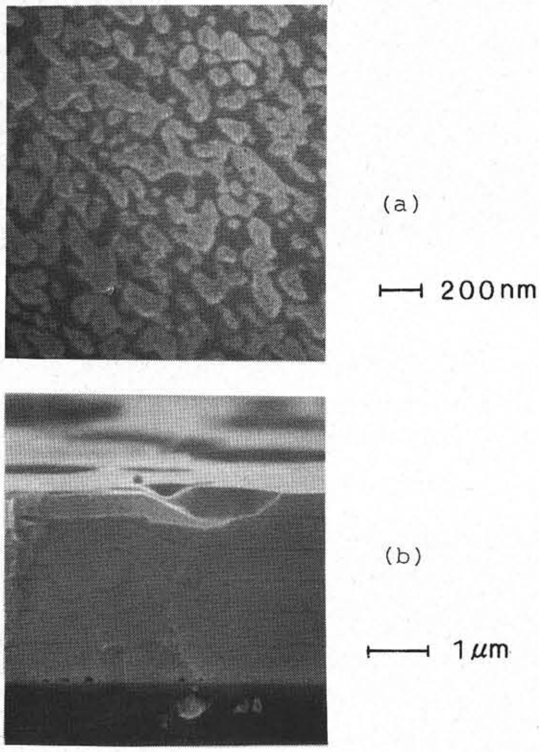


Fig.6 Plane view SEM image of the GaAs buffer layer after the thermal cycle (a) and cross-sectional SEM image of the GaAs layer (marked with AlGaAs thin layers) grown on the island-like shape buffer layer (b).

indicates that the thermal cycle has the effect of stopping the propagation of twins through epitaxial layers. The introduction of defects on the top end of twins in the buffer layer by the thermal cycle can explain these results, but further investigations are needed to clarify the mechanism.

The surface morphology of the buffer layer before and after the thermal cycle were also studied by SEM. The buffer layer which was grown on Si at low temperature had a smooth surface,before the thermal cycle. But, after the thermal cycle (annealed above 750 °C), it occasionally showed island-like ununiformities (Fig.6 (a)). The degree of this change of crystallization was influenced by the anneal temperature, the V-III ratio and the temperature of the buffer layer growth. The GaAs layer grown on such an island-like buffer layer shows an anomalous growth (Fig.6 (b)) and has a lot of pits on its surface. On the other hand, the layer grown on the uniform buffer layer has a very smooth surface.

4.CONCLUSION

GaAs layers with smooth, specular surfaces without scale-like steps were grown on (001) just Si substrates by MOCVD using a thermal cycle treatment of the buffer layer. This treatment has large effects on the growth of GaAs on Si; causing the elimination of anti-phase defects, the interruption of propagation of twins originating from the GaAs/Si interface and the decrease of EPD from $5\times10^{8}cm^{-2}$ to $3\times10^{7}cm^{-2}$. The observations of the surface morphology of the buffer layer before and after the thermal cycle show that the growth of GaAs layers with the smooth and specular surfaces require the uniform buffer layers.

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