

The Growth of GaAs on Recrystallized Ge/SiO₂/GaAs

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GaAs SOI process was studied. Pseudo-line shaped electron beam annealing method with trapezoidal modulation was applied for lateral seeding epitaxy of Ge on SiO₂ using SrF₂ seeding layer, and single crystalline Ge regions as large as 0.3mm×0.8mm were successfully obtained. SOI-GaAs grown by MOCVD on the SOI-Ge layer was proved to be (100) single crystal with good surface morphology. Diffusion of Ge into the GaAs layer grown by MOCVD was up to 0.6 μm, which showed the possibility of fabricating devices on the SOI-GaAs layer.

1.Introduction

The epitaxial growth of semiconductors on amorphous insulators (SOI) has attracted very large interest in terms of three dimensional (3-D) devices in recent years, however, only a few attempts have been made for the GaAs SOI, which can bring forth a new type of application such as the monolithic integration of high-speed devices and opto-electronic devices.

To grow GaAs epitaxially on amorphous insulators, it is an effective method to first recrystallize Ge on insulators by lateral seeding epitaxy, then grow GaAs on the Ge layer. In earlier works, insulator-coated Si was used as a substrate and graphite strip heater⁽¹⁾ or laser beam annealing method⁽²⁾ were used for the Ge SOI process.

We studied the Ge SOI process on a GaAs layer for the purpose of GaAs multi-layered structure and found epitaxial SrF₂ works as a superior seeding material. For the lateral seeding epitaxy of Ge, we applied pseudo-line shaped electron beam (PL-EB) annealing method with trapezoidal modulation for the first time. GaAs was then grown by MOCVD on the recrystallized Ge,

yielding GaAs SOI structure.

In this report, the Ge SOI process and the evaluation of the SOI-GaAs layer are described. The diffusion of Ge into the grown GaAs layer is then investigated from a viewpoint of device fabrication.

2.Experiment

A cross-sectional view of the sample is shown in Fig.1.

SrF₂ seeding layer of 1500 Å was epitaxially grown on an (100)-oriented GaAs wafer by MBE. SrF₂ has almost the same lattice constant as GaAs or Ge^(3,4) and the epitaxial growth of Ge/SrF₂/GaAs is easily obtained. Moreover, SrF₂ is a good insulator and thermally stable, which is favorable to the purpose of GaAs SOI process. CVD SiO₂ of 3000 Å was then deposited and W of 500 Å was sputter-coated to improve wetting characteristics for Ge⁽⁵⁾. After the SiO₂ and W were etched by reactive ion etching(RIE) to form seeding areas, Ge of about 8000 Å was deposited by MBE at the substrate temperature so as to be epitaxially grown on the SrF₂ seeding areas. To encapsulate Ge during the annealing process, sputtered W of 1000 Å, CVD SiO₂ of 1 μm and W of 500 Å

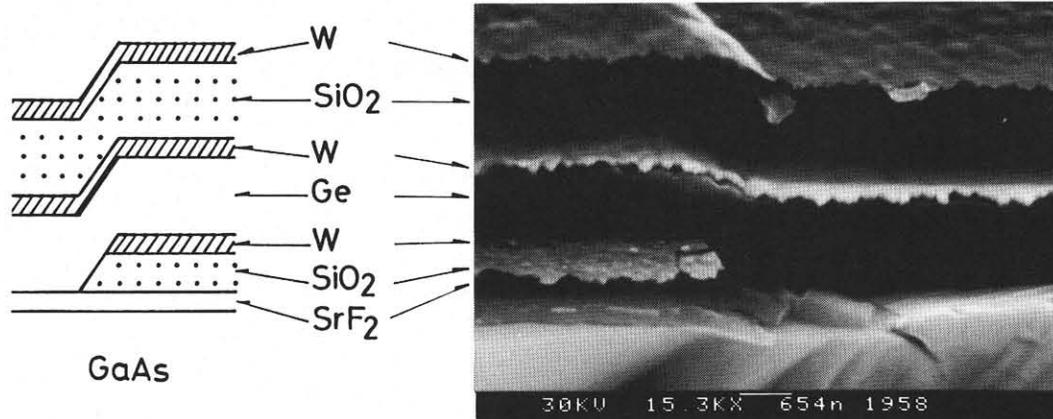


Fig.1 Cross-sectional view of sample for Ge SOI process

were deposited in sequence. This three-layered capping configuration was very effective to prevent the agglomeration of Ge.

The Ge was recrystallized by the PL-EB annealing, which may be the most advantageous for the GaAs 3-D process because it is easy to control the temperature profile of annealed areas and heating depth, which is closely related to the thermal damage to devices under the Ge layer, by the scanning method and the acceleration voltage of electron beam. Typical conditions of the PL-EB annealing are tabulated in Table 1.

Table 1 Conditions of PL-EB annealing

Parameter	Typical value
Acceleration voltage	20 kV
Beam current	1.7-1.9 mA
Beam diameter	100 μm
Modulation wave form	Trapezoidal
Modulation frequency	1 MHz
Beam oscillating width	0.6 mm
Scanning speed	1 m/s
Substrate temperature	700 $^{\circ}\text{C}$

Optimizing the wave form of trapezoidal modulation, uniformly recrystallized regions of about $0.8\text{mm} \times 0.3\text{mm}$ were obtained at the modulation frequency of 1MHz, the scanning speed of 1m/s, the beam oscillating width of 0.6mm and the acceleration voltage of 20kV.

After the annealing, the capping layers were removed by RIE for W and buffered-HF for SiO_2 , and GaAs was grown by MOCVD on the Ge layer.

3. Results

Fig.2 shows Raman spectra of Ge which were just deposited and annealed on SiO_2 .

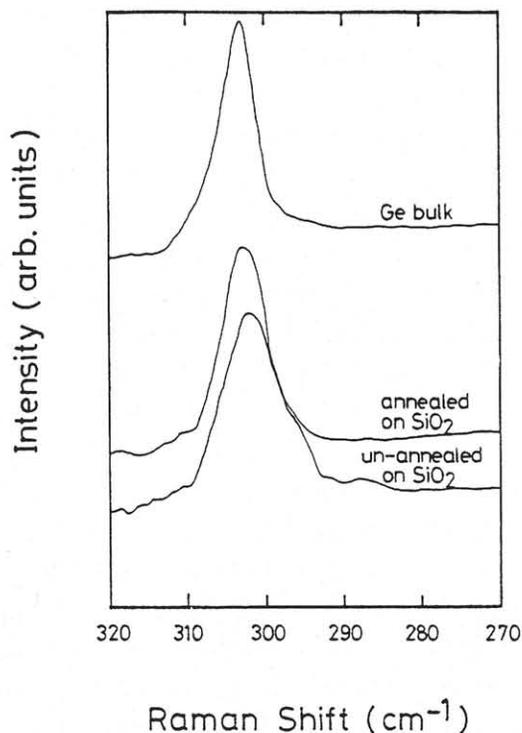


Fig.2 Raman spectra of Ge

Table 2 Raman data

Sample	Peak shift (cm^{-1})	Half width (cm^{-1})	Stress ($\text{dyn} \cdot \text{cm}^{-2}$)
Bulk Ge	----	5.0	----
Ge on SiO_2 unannealed	-0.8	8.0	2.7×10^9
annealed	-0.5	6.3	1.7×10^9

The spectrum of bulk Ge is also shown for reference. From the half width of the spectra as listed in Table 2, the crystallinity of the recrystallized Ge was clearly shown to be comparable to that of bulk Ge.

Stress($\text{dyn} \cdot \text{cm}^{-2}$) in Ge layer can be calculated from $3.4 \times 10^9 \omega^{(6)}$, where $\omega(\text{cm}^{-1})$ is a peak shift. As listed in Table 2, the stress of the recrystallized Ge was tensile stress of $1.7 \times 10^9(\text{dyn} \cdot \text{cm}^{-2})$, which was about one third of the recrystallized Ge on an insulator-coated Si substrate as was reported in the previous work.⁽⁶⁾

GaAs of about $2 \mu\text{m}$ was then grown on the Ge layer by MOCVD using two-step growth technique. Fig.3 is a cross-sectional view of GaAs grown on unannealed areas.

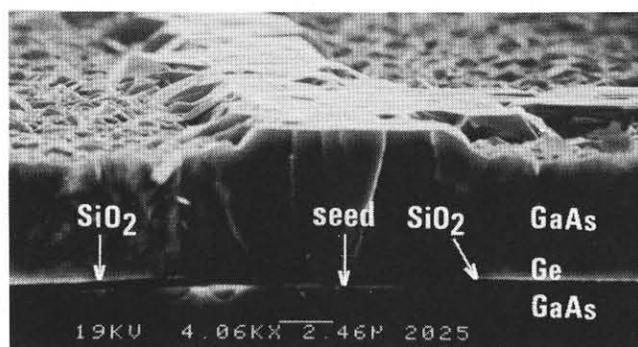


Fig.3 Cross-sectional view of GaAs grown on unannealed Ge

It is clear that single-crystalline GaAs was grown on the SrF_2 seeding area, while poly-crystalline GaAs grown on SiO_2 area and the growth rate for each area was not equal. Fig.4 is a cross-sectional view of GaAs grown on the recrystallized area.

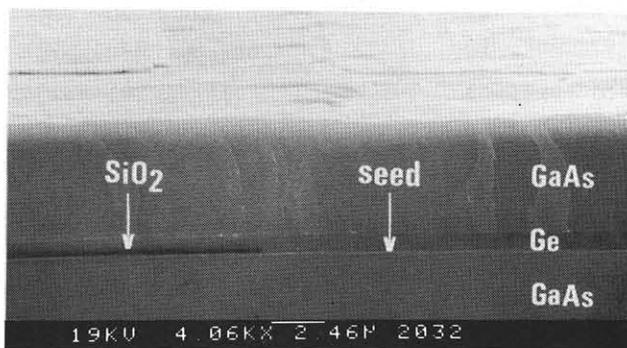
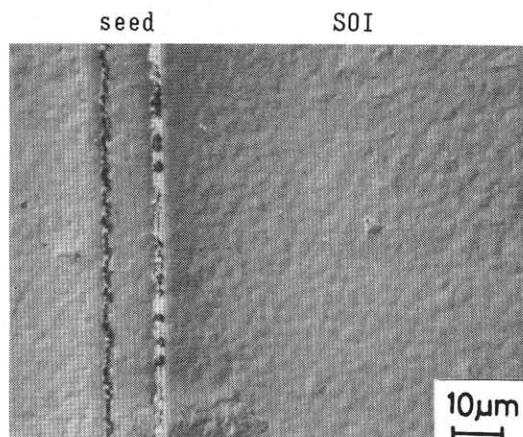


Fig.4 Cross-sectional view of GaAs grown on recrystallized Ge

The surface is fairly smooth and seems to be enough for device fabrication process. Fig.5 (a) shows Nomarski micro-photograph and (b) shows electron channeling pattern (ECP) of the SOI-GaAs surface.



(a) Nomarski microphotograph of SOI-GaAs surface

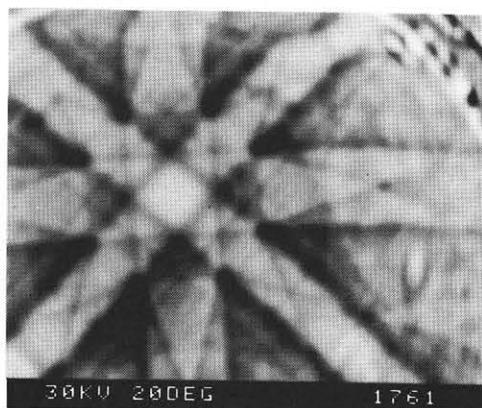


Fig.5 (b) ECP of SOI-GaAs

By the surface morphology and the four-fold symmetry in ECP, the SOI-GaAs was proved to be (100) single crystal, of which crystal orientation was inherited from the GaAs substrate.

The diffusion of Ge into the GaAs layer grown by MOCVD using two-step growth technique was analyzed by means of secondary ion mass spectrometry (SIMS). Fig.6 shows depth profile of Ge in the GaAs grown at 650°C on the MBE Ge/(100)GaAs substrate.

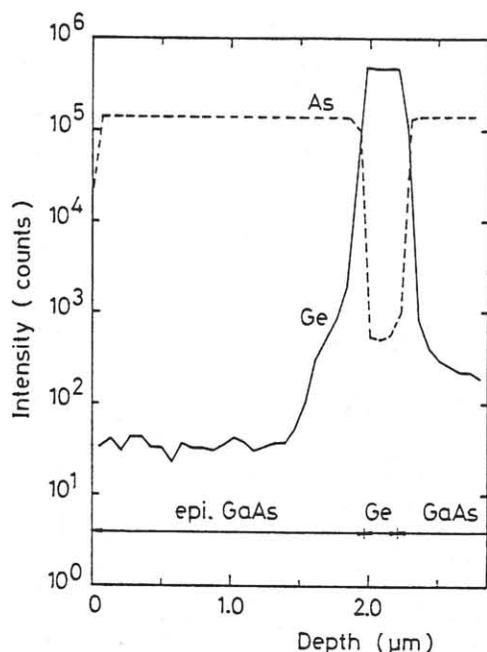


Fig.6 SIMS profile of Ge in GaAs grown by MOCVD

It was estimated that the diffusion of Ge amounts to about 0.6 μm from the GaAs/Ge interface at this growth temperature. When the grown layer was thicker than about 0.6 μm, crystal properties of the upper part of the layer were determined by the growth condition such as a V/III ratio or intentional doping, and using V-doped GaAs buffer layer, semi-insulating GaAs layer, which is indispensable for the device fabrication, was successfully grown on the recrystallized Ge layer.

4. Conclusion

By PL-EB annealing method with trapezoidal modulation, Ge was successfully

recrystallized on SiO₂ using SrF₂ seeding layer epitaxially grown on GaAs for the first time. Single crystalline GaAs of (100) orientation was grown by MOCVD on the recrystallized Ge. Diffusion of Ge into the grown GaAs layer was up to 0.6 μm, which showed the possibility of fabricating devices on the SOI-GaAs layer.

These results were to promise the realization of GaAs 3-D devices.

5. Acknowledgement

This work was performed under the management of the R&D Association for Future Electron Device as a part of the R&D Project of Basic Technology for Future Industries sponsored by the Agency of Industrial Science and Technology, MITI of Japan.

6. References

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