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MOS-FETs Fabricated by SPE-SOI Technology

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Electrical characteristics of Si layers on SiO_2 obtained by seeded-lateral Solid Phase Epitaxy were evaluated as a function of distance from the seeding area. According to the two growth modes in lateral epitaxy, it was found that there are significant difference in the electrical characteristics of MOSFETs fabricated in those regions. A field effect (electron) mobility of about 700cm^2/Vs was obtained for n-channel MOSFETs fabricated in the {110}-facet grown region. However, the electrical properties of MOSFETs fabricated in the {111}-facet growth region were not as good. The results suggest that the {110}-facet growth region is suitable for devices with a feature size of less than 2μm.

1. Introduction

Silicon-on-insulator (SOI) structures have been investigated intensively to realize 3-dimensional structures in an attempt to realize high speed, high packing density, and multi functions. Several methods of realizing SOI structures have already been proposed, such as liquid phase epitaxial re-growth of polycrystalline silicon using laser beam[1] or electron beam[2] irradiation, and buried oxide formation with oxygen ion implantation (SIMOX)[3]. In fabricating 3-dimensional devices, it is extremely important not to affect the underlying device structure either thermally or mechanically. From this viewpoint, a low temperature process is required for the SOI process. One suitable technology is lateral solid phase epitaxial (L-SPE) growth. In this technology, an amorphous Si layer on an insulator is converted into single crystal silicon by epitaxial growth in the solid phase.

As the process can be carried out at a relatively low temperature around 600℃, it can be regarded as the most promising method for fabricating devices on top of underlying devices covered by insulators.

So far, several reports have appeared on L-SPE concerning the dependence of the growth length of the single crystalline area on crystallographic orientation[4-5], the cross sectonal TEM observation of the grown region[6-7], impurity-enhanced crystal growth in L-SPE[8], and so on. However, very little has been reported about the electrical characteristics of the grown area[9-10].

The present paper describes the characterization of n-channel MOSFETs fabricated in an SOI structure formed by L-SPE. The discussion focuses especially on the relation between electrical characteristics and the crystallinity.

2. SOI Formation by L-SPE

A p-type, (100)Si(8-12Ω cm) wafer was used as the starting material. The substrate was coated with 200nm-thick thermal SiO_2 arranged in stripe patterns. The patterns were formed perpendicular to

the <100> direction, which was the direction of the longest L-SPE growth. The substrate surface were cleaned prior to a-Si deposition using low energy Ar-ion beam sputtering with N_2 annealing at 680℃ (60min). After surface cleanning, an a-Si layer was formed by electron beam deposition in an ultra-high vacuum ($<2x10^{-7}$Pa) to a thickness of 0.45-0.6μm. Then the a-Si layer was annealed at 450℃ in ultra-high vacnum. L-SPE of the a-Si layer was carried out by N_2 annealing at 600℃.

Single crystal growth length is shown in Fig. 1 as a function of annealing time. Single crystal growth occurs first vertically from the substrate surface in the {100}-facet growth mode and then laterally after over-riding the edge of SiO_2 pattern. There are two growth modes, in the lateral growth direction. The first is facet growth in the {110} direction followed by facet growth in the {111} direction which continues until L-SPE stops.

The existence of such a growth mode has already been reported[5]. In the case of Fig. 1, the growth length was 2.5μm for both the {110}-facet growth region and the {111}-facet growth region. Given this background, the annealing period for MOSFET fabrication was determined to be 7Hrs.

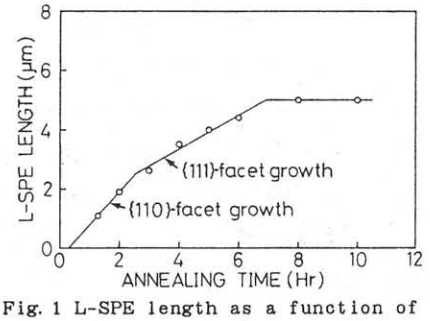

Fig. 1 L-SPE length as a function of annealing time.

3. Fabrication of SOI-MOSFETs

The MOSFETs shown in Fig. 2 were fabricated on SOI structures formed by the processes mentioned above.

After the etch-off device isolation process which leaves the SOI layer for MOSFET fabrication, B-ions were implanted (30keV, $3X10^{11}cm^{-2}$) to make the SOI layer p-type for nMOS fabrication. MOSFETs (gate oxide thickness; 35nm) were then fabricated by means of the conventional poly-Si gate nMOS fabrication process. The gate length and the gate width of the MOSFETs was 1-10μm and 4-10μm, respectively.

To evaluate the electrical properties of the SOI layers, MOSFETs were fabricated in a grown layer by changing the location of the channel region.

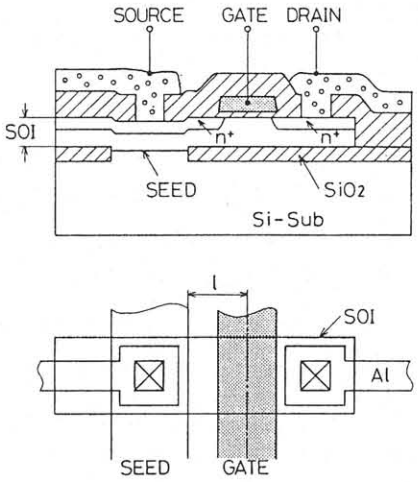

Fig. 2 The structure of the SOI MOSFET.

4. Electerical characteristics of SPE-SOI MOSFETs

Drain current-drain voltage (Id-Vd) characteristics are shown in Fig. 3 as a function of distance (l) between the edge of the seeding region and the center of the gate. Distance (l) was varied from 1 to 6μm. The electrical characteristics of MOSFETs fabricated within 2μm from the seed edge are quite ordinary and very much comparable to those for bulk MOSFETs. However, in the case of l larger than 3μm, the fabricated MOSFETs showed an abnormal function. Subthreshold drain current, measured at a drain voltage and a gate voltage are 5V and 0V, respectivery,

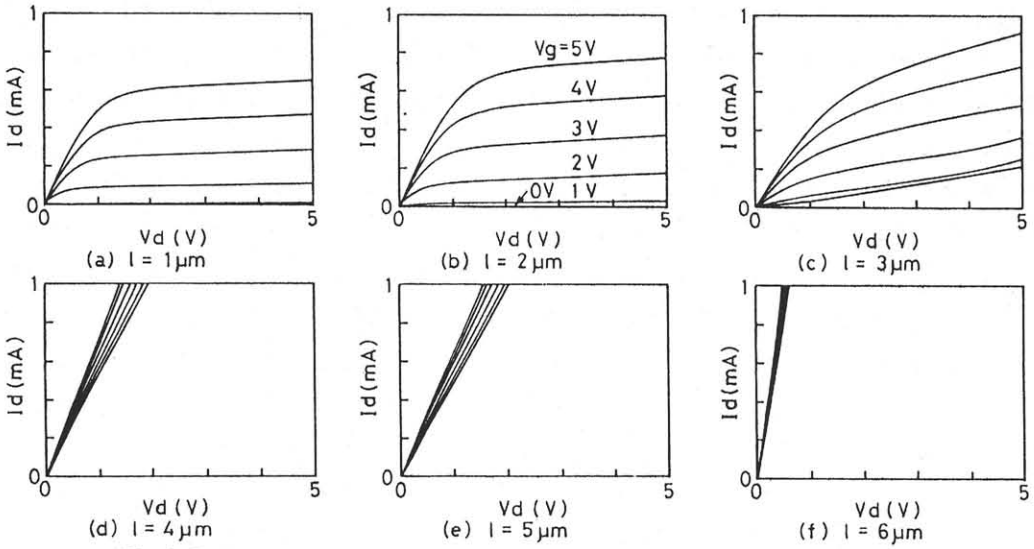

Fig. 3 Id-Vd characteristics of MOSFETs as a function of the distance between the edge of the seeding region and the center of the gate.

is plotted as a function of l, and the results are shown in Fig. 4. The figure also shows that leakage current in the {111}-facet region and in the polycrystalline region is very much larger than that in the {110}-facet growth region. These results correspond to the facet growth mode, and only the MOSFETs fabricated in the {110}-facet growth region operate normally.

Two main reasons can be considered for the increase in leakage current. One is the increase in carrier generation-recombination velocity in the junction area due to an inferior crystallinity in the vicinity of the channel region. The other is the possibility of an electrical short-circuit between the source and drain, arising as a result of enhanced inpurity diffusion, which was caused by high density crystal defects (micro twins)[4] in the {111}-facet region and at grain boundaries in the polycrystalline region, during thermal processes.

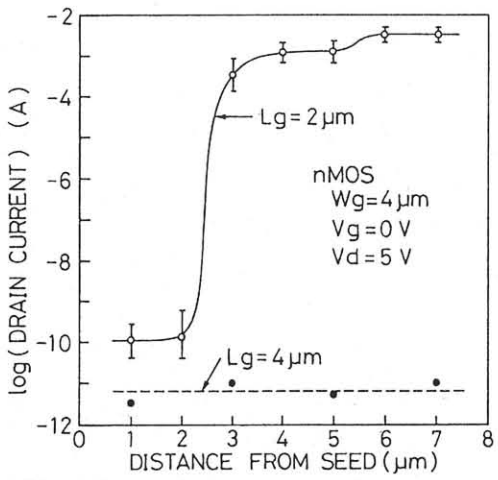

Fig. 4 Leakage current as a function of the distance from the seed edge.

To clarify the reason, leakage current dependence on l was measured for MOSFETs with a long gate length (4μm). These MOSFETs are not influenced by even a rather large redistribution of impurities in the source and drain regions. The results are also shown in Fig. 4 in contrast with those for the 2μm gate. The leakage current level is low compared with that for the 2μm case, and does not show l dependence with increasing distance from the seeding area. The result clearly shows that leakage current is not due to recombination centers but due to a drain-source short-circuit which originates from the enhanced impurity diffusion.

Transconductance (g_m) was measured under a drain voltage of 0.1V. The result is plotted against l and is shown in Fig. 5. The figure shows that g_m is almost constant at approximately 26μS when l is less than 2μm. This value corresponds to a field effect mobility of 720cm^2/Vs.

However, g_m decrease to 10μS when l becomes larger than 3μm. This indicates that g_m characteristics, as well as leakage current characteristics, degrade in the {111}-facet growth region. With respect to the subthethold characteristics of MOSFETs fabricated in the {110}-facet growth region, the leakage current (drain current) at a drain voltage of 5V and at a gate voltage of OV was measured to be 5×10^{-11}A/μm, and tailing factor was 85mV/dec. These values were obtained for more than 80% of the devices fabricated on a 100mm diameter Si wafer.

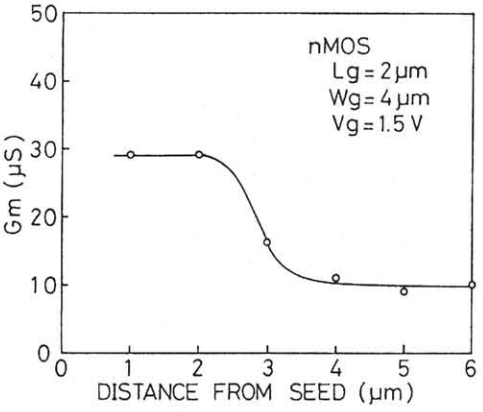

Fig. 5 Transconductance(g_m) as a function of the distance from the seed edge.

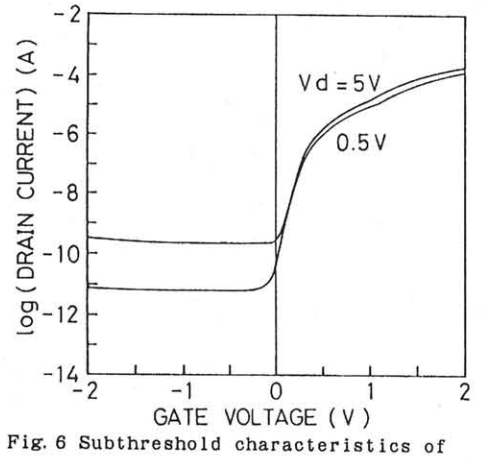

Fig. 6 Subthreshold characteristics of MOSFETs fabricated in the {110}facet growth region.

5. Conclusion

The electrical characteristics of n-cannel MOSFETs fabricated in the L-SPE SOI region were investigated. The differences in electrical characteristics between the growth modes in L-SPE were distinctive. MOSFETs fabricated in the {111}-facet growth region have low channel mobilities and high leakage current. On the contrary, the electerical characteristics of MOSFETs grown in the {110}-facet growth region were shown to be quite suitable for LSI applications.

SOI structures formed by L-SPE in the {110}-facet growth direction is expcted to play an important rule in novel 3-dimensional device structures.

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