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SOI Recrystallization using a Multiply Separated Seed Structure

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An improved seed structure, a multiply separated seed structure, in which dot seeds along a line are formed in tapered insulating layer, has been demonstrated for smoothly melting without void in both seed and field SOI region. This seed structure has been verified to be useful for laterally seeded epitaxial recrystallization of SOIs without slip generation in silicon substrate as compared with conventional seed structures.

1. Introduction

Electron beam annealing technologies for silicon on insulator (SOI) technology have been extensively investigated, and amplitude modulated pseudo-line electron beam (AMPL-EB) technique[1] has been proposed for large area chip size SOI.

The crystallographic orientation control for SOI is also very important for device applications. Therefore, laterally seeded epitaxy has been studied to obtain high quality SOI. However, voids are often generated at a seed region by a steep temperature gradient near the seed, and melting the seed is critically affected by insulating layer thickness. In order to improve these problems, the various seed structures have been proposed[2,3,4].

A perforation seed structure[2], in which rectangular seed regions are separately arranged along a line, has been reported to be useful for void suppression at the seed region by reduction of seed opening area.

From a viewpoint of stacked device application, both a thick insulating layer (> 2 μm) and minimization of beam energy for seed melting is necessary to avoid slip generation in underlying devices during the recrystallization of SOIs. A partially thickened SOI (PTS) seed structure[4] has been reported to be useful for melting the seed region in silicon films on thick insulating layer.

This paper reports an improved seed structure, a multiply separated seed (MSS) structure, in which dot seed (1.2 μm in diameter) along a line are formed in tapered insulating layer and silicon film was thickened as compared with SOI region. This structure proved to be effective to recrystallize silicon films on thick insulating layer (2.5 μm) without void generation at the seed region and slip generation in silicon substrate.

2. Void suppression

AMPL-EB annealing was employed with

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10 kV acceleration voltage, 1 mm beam width, 100 mm/s beam scan velocity and 750 ℃ substrate temperature.

Figure 1 shows a multiply separated seed structure. A dot seed, as shown in Fig. 1, is 1.2 μm in diameter and 0.8 μm deep. At the seed region, SOI thick is 1.2 μm. At SOI field region, SOI thick is 0.8 μm. A capping and insulating layer are 0.5 μm and 2.5 μm thick silicon dioxide films, respectively.

Figure 2 shows that a void was generated at the seed region with 2.4 μm dot seed interval in crystallization process. The voids might be generated by sudden silicon volume contraction in rapid melting[5] process near the seed region.

It seems that equilibrium (1) among liquid silicon, solid silicon dioxide and silicon monoxide gas can be nearly reached in a void.

$$Si(l) + SiO_2(s) = SiO(g) \qquad (1)$$

$$P_{SiO} = EXP\ (\Delta G\ /\ -\ R\ T\ ) \qquad (2)$$

where P_{SiO} is SiO gas pressure, ΔG is Gibbs free energy changes for reaction (1), R is gas constant, and T is temperature. P_{SiO} is calculated from thermochemical data[6]. At silicon melting point (1685 K), P_{SiO} is 9.8 Pa. Even at 1800 K, about 100 K above the melting point of silicon, P_{SiO} is 167 Pa. The total pressure in a void is mainly silicon monoxide pressure, according to equilibrium calculation. These pressure values seem to expand the void under vacuum, as shown in Fig. 2. Moreover, the void expansion is determined by silicon surface tension.

$$P = 2\ \gamma\ /\ r \qquad (3)$$

Where P is equilibrium pressure in the void, γ and r are surface tension of silicon[7] and radius of void, respectively. Equation (3) suggest that the equilibrium radius of void is 8.6×10^3 m even at 1800 K.

Thus, the reaction occurred at the molten zone, but small void below silicon film thickness is extinguished by silicon surface tension. Therefore, in order to suppress the void generation, decreasing temperature gradient at seed region is required.

Figure 3 shows that the void generation was suppressed with increasing the dot seed interval, because of

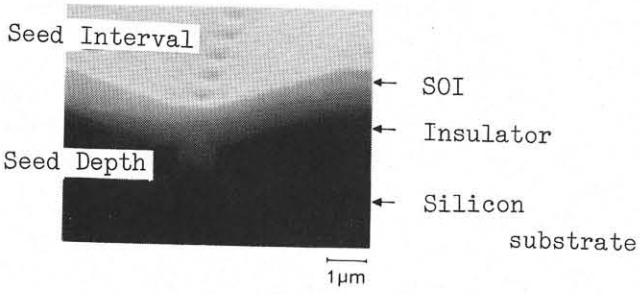


Fig.1 Multiply separated seed structure.

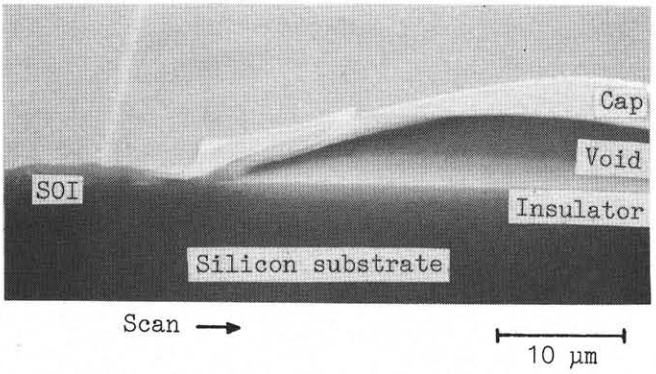


Fig.2 SEM photograph of void in seed region.

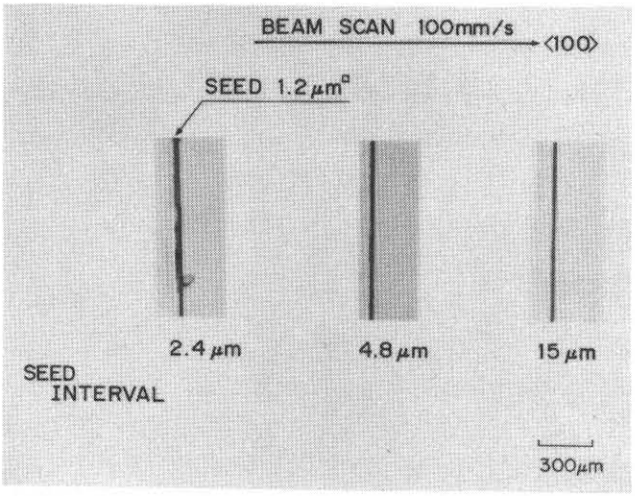


Fig.3 Voids generation in MSS structure with various dot seed interval.

increasing heat conduction from the seed region to the silicon substrate.

The MSS structure with seed interval wider than 15 μm was sufficiently suppressed void generation. In the case of seed interval wider than 20 μm, however, sub-grain boundary were observed between adjacent dot seeds after recrystallization and preferential etching. Therefore, the optimum seed interval is 15 μm.

Using the MSS structure, the seed region is melted with 6.0 mA beam current. Figure 4 shows a Nomarski optical microscope photograph of a recrystallized SOI layer. Preferential etching and pit grid etching shows that the SOI crystallographic orientation is well controlled by the (100) seed.

3. Slip generation in the silicon substrate

Figure 5 shows a slip in the substrate with devices after SOI recrystallization. The sample is prepared by Wright etching after SOI and insulator removal.

The relationship between electron beam current and observed slip length in the substrate is shown in Fig. 6. At 100 mm/s beam scan velocity and 6.0 mA electron beam current, SOI can be melted without slip in the substrate.

Seed region in the MSS structure is melted with 6.0 mA beam current, as shown in Fig. 4.

However, conventional perforation seed (1.2 μm in diameter and 2.5 μm deep), and PTS line seed (1.2 μm width) is not

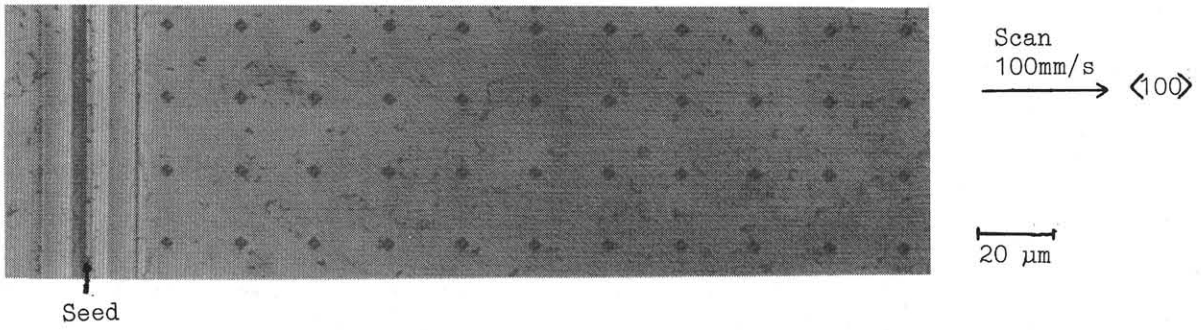


Fig.4 Nomarski microscope photograph of recrystallized SOI with MSS structure by 6.0 mA electron beam current after preferential etching. Etch-pit grid method was carried out to evaluate crystallographic orientation.

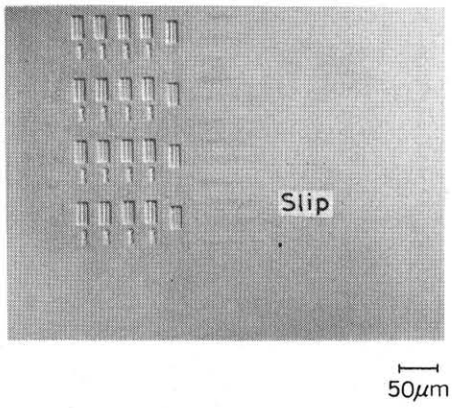


Fig.5 Microscope photograph of slip in substrate fabricated device after Wright etching.

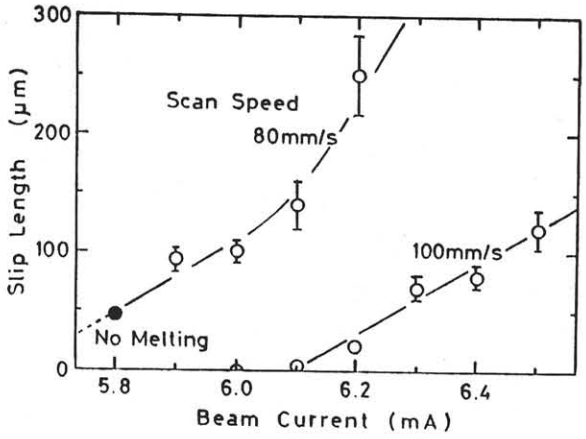
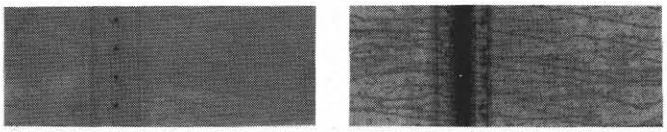


Fig.6 Relation between substrate slip length and electron beam current for SOI recrystallization.

melted with 6.0 mA beam current, as shown in Fig. 7. Grain boundaries across the seed region are clearly shown by preferential etching.



Dot seed (1.2 μm diameter and 2.5 μm deep) PTS line seed

20 μm

Fig.7 Microscope photograph of recrystallized SOI with dot seeds (1.2 μm diameter and 2.5 μm deep) and a PTS line seed by 6.0 mA electron beam current after preferential etching.

The MSS structure can be melted easier than the conventional perforation seed, for the following two reasons.

First, tapered insulating layer and thickened SOI in MSS structure assists seed melting by lateral heat conduction around the seed.

Second, calculated value[8] for deposited electron energy in silicon at 10 kV acceleration voltage suggests that the interface between SOI and substrate for the MSS structure (seed depth 0.8 μm) is heated more directly by electron beam than that for conventional perforation seed (2.5 μm deep, that is insulator thickness).

Therefore, the seed region is very easily melted at the MSS structure.

4. Conclusion

An improved seed structure, a multiply separated seed structure, in which dot seeds along a line are formed in tapered insulating layer and silicon film was thickened as compared with SOI region, has been demonstrated for smoothly melting without void in both seed and field SOI region.

Laterally seeded epitaxy of silicon films on thick insulating layer (2.5 μm) without void and sub-grain boundary generation is attained by optimizing dot seed (1.2 μm in diameter) interval, 15 μm.

It is demonstrated that the beam current to melt seed region in this seed structure is minimized in comparison with that in conventional seed structure. This enable to suppress the slip generation in silicon substrate with 100 mm/s beam scan velocity.

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Reference

(1)T.Hamasaki, T.Inoue, I. Higashinakagawa, T.Yoshii, and H.Tango, J.Appl.Phys. 59 (1986) 2971.

(2)S.Horita and H.Ishiwara, Appl.Phys.Lett. 50 (1987) 748.

(3)S.Kusunoki, K.Sugahara, T.Nishimura, T. Kumamoto, M.Nakaya, N.Yazawa, and Y. Horiba, Symposium on VLSI Tech. (1987) 107.

(4)T.Hamasaki, T.Inoue, M.Yoshimi, T. Yoshii, and H.Tango, SOLID STATE DEVICES AND MATERIALS,The 18th Conf. (1986) 569.

(5)T.Inoue and T.Hamasaki, Appl.Phys.Lett. 13 (1987)

(6)JANAF Thermochemical Tables. NSRDS-NBS. 1971.

(7)C.L.Yaws, L.L.Dickens, R.Lutwack, and G.Hsu, Solid State Technol., January, (1981) 87.

(8)A.Neukermans and W.Saperstein, J.Vac. Technol., 16 (1979) 1847.