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The Effect of Charge Build-up on Gate Oxide Breakdown during Dry Etching

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The effect of charge build-up on gate oxide breakdown was studied using a barrel type dry etcher. The charging polarity during dry etching depended on the direction of a wafer in the barrel chamber. In the case of negative charge build-up, gate oxide breakdown occurred more frequently with thinner gate oxides. For positive charge build-up, on the other hand, no gate oxide breakdown was observed in the samples with thicknesses of more than 4nm. Moreover, the gate oxide breakdown was found to depend on a pad poly Si connected to gate. These results are explained with the currents from plasma to Si substrate through gate oxide.

1. Introduction

In VLSI fabrication, MOS devices are damaged during dry etching because of exposure to plasma, causing gate oxide breakdown.[1)2)] This problem will be more serious as gate oxide becomes thinner for further miniturization of MOS devices.

Gate oxide breakdown during dry etching depends on gate oxide thickness, device structure, charging polarity and the amount of charge on gate electrodes. The charge build-up varies with the structure of an etcher and etching conditions.

This paper presents the effect of charge build-up on gate oxide breakdown during O_2 plasma treatment using a barrel type dry etcher. The amount of charge build-up on gate electrodes was evaluated as the flat band voltage shift (ΔV_{FB}) of metal / silicon nitride/ silicon dioxide/ silicon (MNOS) capacitor loaded in the chamber as a monitor.[2)] The gate oxide breakdown during plasma treatment was checked for two different structures of MOS capacitors. Moreover, the relation between charge build-up, especially polarity, and gate oxide breakdown is discussed.

2. Experiment

2.1 Dry Etching Equipment

A barrel type etcher was used through all experiments. A Si wafer was set in two ways as shown in Fig.1; (a) perpendicular to electric fields (W⊥E) and (b) parallel (W//E). All samples were exposed to O_2 plasma at a pressure of 2.5torr and an rf power of 400W for 20 minutes.

2.2 Charge Build-up

In order to evaluate the charge build-up on gate electrodes, an MNOS capacitors were used as shown in Fig.2. Charge build-up is monitored as ΔV_{FB} of the MNOS capacitor.

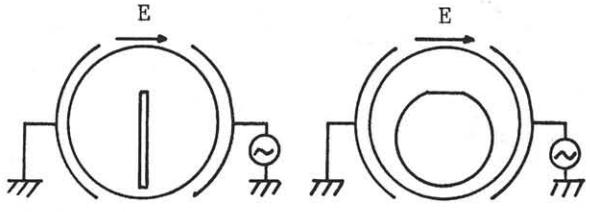


Fig.1 The direction of a Si wafer in the chamber

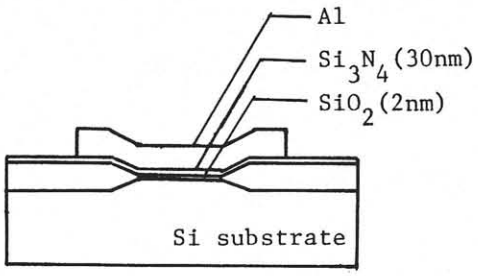
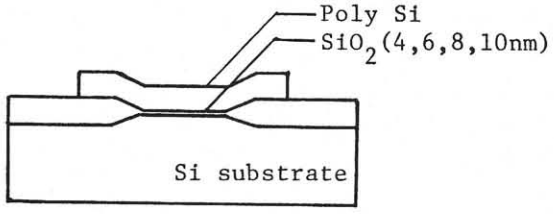
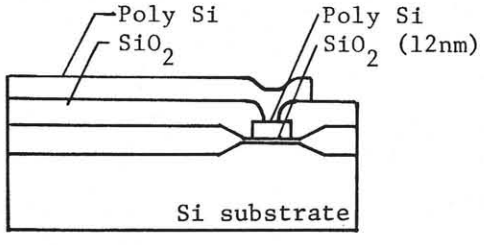


Fig.2 The structure of MNOS capacitor



(a) Sample A



(b) Sample B

Fig. 3 The structure of MOS capacitor

The polarity and amount of charge build-up are relatively defined with respect to Si substrate. When positive charge builds up on the gate electrodes during the plasma treatment, ΔV_{FB} is positive.

2.3 Gate Oxide Breakdown

Two different structures of MOS capacitors were used as shown in Fig.3. Sample A is an MOS capacitor with thin gate oxide ranging from 4nm to 10nm. For these samples the poly silicon gate electrodes were patterned with wet etching, and photoresist was removed with wet etching, to avoid gate oxide breakdown during the sample preparation. The gate area is $1mm^2$. The other sample, B is an MOS capacitor with a large poly Si pad connected to the gate. The area ratios (r) of the pad to gate are $7.1X10^2$, $2.6X10^3$, and $1.4X10^4$. The gate oxide thickness is 12nm, and gate area is $18\mu m^2$.

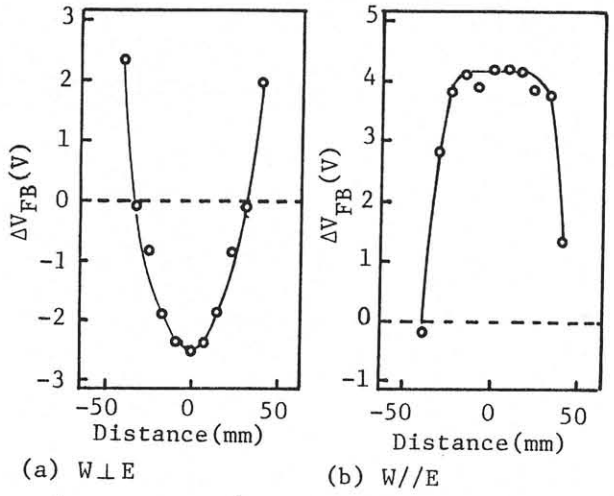


Fig.4 The ΔV_{FB} distributions of MNOS capacitor after the plasma treatment

For these samples, the poly Si patterning and photoresist removement were perfomed by dry etching. No gate oxide breakdown was assured in these samples before the experiments.

3. Result and Discussion

Figure 4 shows the ΔV_{FB} distributions of MNOS capacitors for the two directions in the etching chamber. In perpendicular to electric fields (W⊥E), ΔV_{FB} was negative except near the periphery of the wafer, and the maximum was -2.6V at the center. On the other hand, in parallel to electric fields (W//E), the distribution was almost plateau with a positive value of 4.2V, except near the periphery. The magnitude of charge build-up was larger in W//E than in W⊥E.

Gate oxide breakdown was evaluated for both charging polarities. P and N type Si substrates were used for negative and positive charge build-up, respectively, to accumulate the Si surface of MOS capacitor during the plasma treatment.

Gate oxide breakdown after the plasma treatment was shown in Fig.5. In the sample A with a gate oxide thickness of 6nm, gate oxide breakdown occurred in 15% of MOS capacitors a wafer for negative charge build-up. The broken MOS capacitors concentrated around the center where the

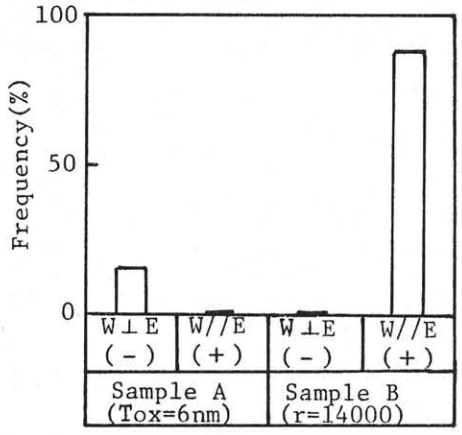


Fig.5 The frequency of gate oxide breakdown

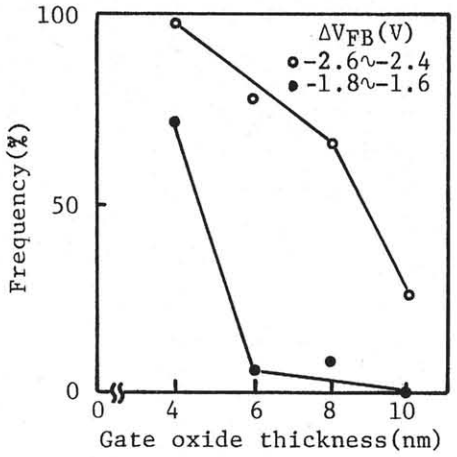


Fig.6 The dependence of gate oxide breakdown on the gate oxide thickness.

charge build-up was maximum. For positive charge build-up, however, no gate oxide breakdown occurred in spite of more charge build-up in magnitude compared with negative charge build-up. On the contrary, in the sample B with poly Si pad area ($r=1.4X10^4$), gate oxide breakdown occurred not for negative charge build-up but for positive charge build-up. In this sample, breakdown was observed all over the Si wafer except near the periphery relating to the ΔV_{FB} distribution.

Figure 6 shows the dependence of gate oxide breakdown on the oxide thickness. In the range of $-2.6<\Delta V_{FB}<-2.4$, the frequency of gate oxide breakdown was more than 50% for oxide thicknesses of less than 8nm. On the other hand, for $-1.8<\Delta V_{FB}<-1.6$, it was less than 10% to the thickness of 6nm and increased to 74% for the thickness of 4nm. Consequently, for negative charge build-up, gate oxide breakdown occurs more frequently with thinner gate oxides depending on the amount of charge. For positive charge build-up, no gate oxide breakdown occurs even if the gate oxide is as thin as 4nm.

Figure 7 shows the dependence of gate oxide breakdown on the area ratio of the poly Si pad to gate in the sample B. For $\Delta V_{FB}>4V$ and $r>2.6X10^3$, all the capacitors were broken down. For $r=7.1X10^2$, the frequency of gate oxide breakdown decreased to 40%, which is considered to further decrease as the area ratio decreases because no oxide breakdown occurred in the sample A corresponding to r=1. Therefore, gate oxide breakdown depends on the area of the conducting patterns connected with the gate electrode, because it collects more charges during the exposure to plasma.

The phenomena related to gate oxide breakdown may be explained as follows. Fig.8 qualitatively illustrates the relation between the gate oxide thickness and the current (Ig) through the gate oxide during the plasma treatment. The shaded part is the

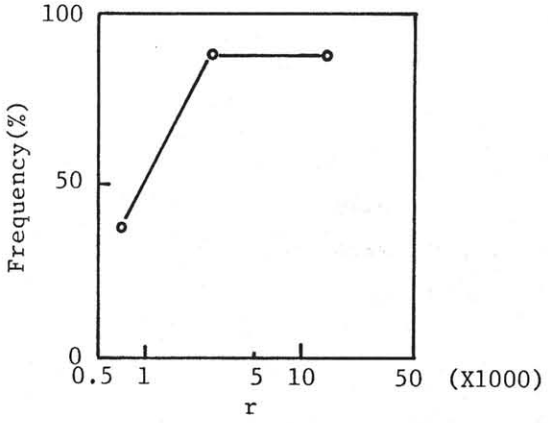


Fig.7 The dependence of gate oxide breakdown on the ratio (r) of the large pad area.

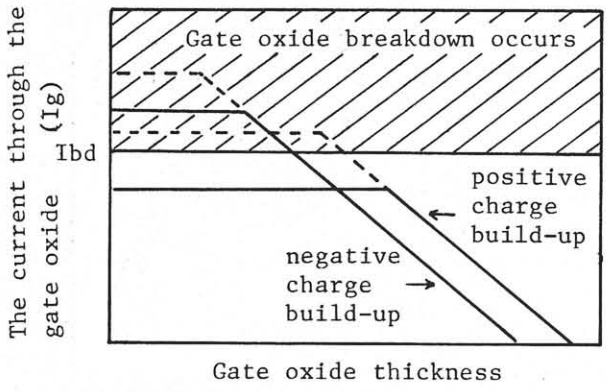


Fig.8 The relation between the gate oxide thickness and the current through the gate oxide

region where gate oxide breakdown occurs, bounded by the critical current Ibd. Ig increases with the decrease of oxide thickness, and eventually reaches to saturation in the thin oxide region, because of the limit of the current supplied by plasma which must be equal to Ig in the steady state.

For negative charge build-up, Ig is limited by the saturation electron current in the thin gate oxide region. Therefore, in this region gate oxide breakdown occurs because the saturation electron current is larger than Ibd. Generally, the saturation ion current is about two orders of magnitude smaller than the saturation electron current. Therefore, no gate oxide breakdown occurs for positive charge build-up in any oxide thickness because the saturation ion current is smaller than Ibd.

The effect of the large poly Si pattern connected to the gate as in the sample B is that the current supplied to the gate electrode increases in proportion to the poly Si pattern area. Therefore, the current to limit Ig becomes larger as shown in Fig.8 (dushed lines), and gate oxide breakdown occurs for positive charge build-up. In sample B no gate oxide breakdown occurred for negative charge build-up as shown in Fig.5. This is because the gate oxide is too thick for negative charge build-up which is smaller in magnitude than positive charge build-up.

4. Conclusion

In a barrel type etcher, the polarity of charge build-up during the plasma treatment depends on the direction of a Si wafer with respect to electric fields, i.e. in parallel to electric fields, gate electrodes are charged up positively, and in perpendicular, they are charged up negatively.

The following facts are found about gate oxide breakdown during dry etching with the barrel type etcher.

(1) For negative charge build-up, gate oxide breakdown occurs when the oxide thickness becomes thinner.

(2) For positive charge build-up, no gate oxide breakdown occurs in any oxide thichness.

(3) When a large conducting pattern is connected to the gate electrode, gate oxide breakdown occurs even for positive charge build-up.

A simple model is presented to successfully explain the phenomena respect to gate oxide breakdown by charge build-up during the plasma treatment.

Acknowldgment

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References

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(2) Y.Kawamoto, CSSDM, Tokyo p333(1985)