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Highly Reliable Ta_2O_5/SiO_2 Double Dielectric Films on Poly Crystalline Silicon

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Highly reliable Ta_2O_5/SiO_2 double dielectric films on poly-Si, having an effective film thickness of 4~5 nm SiO_2, are developed. The bottom SiO_2 is grown by dry oxidation through reactively sputtered Ta_2O_5 film at temperature higher than 800℃. The growth rate of the bottom SiO_2 is controlled by the diffusion of oxydant through Ta_2O_5 film, so that the uniform oxidation is performed resulting in high quality bottom SiO_2. The TDDB characteristics show that these double dielectric films with thinner bottom SiO_2 are more resistant to breakdown. Films with 2nm bottom SiO_2 have more than 4 decades longer lifetime to breakdown than thermally grown SiO_2 on single crystalline Si and have a low leakage current of 10^{-8}A/ cm^2 at 5MV/cm.

INTRODUCTION

As the level of integration in VLSI's become increasingly higher, the area of capacitors become correspondingly small. However, this reduction in capacitor area reduces capacitance, leading to lower reliability of memory devices. To overcome this limitation, three-dimensional device structures, such as trenched or stacked type capacitors have been proposed to reduce memory cell area (1, 2). At the same time, a means has already been proposed in which an oxide of a transition metal having a relatively large dielectric constant is employed as the dielectric film in the capacitor in order to prevent lowering of capacitance(3).

It is clear that the application of dielectric film with a large dielectric constant to three dimensional devices is expected to greatly reduce the memory cell area. However, the dielectric film of three dimensional devices must be formed on poly-crystalline silicon (poly-Si) film. Hence, high reliability must also be ensured in the application of dielectric film with large dielectric constant, such as Ta_2O_5.

SAMPLE PREPARATION

The fabrication process of the W-gate/Ta_2O_5/SiO_2/poly-Si capacitor investigated in this work is shown in Fig. 1(a-c). In (a), a poly-crystalline silicon film is deposited on a (100) n-type Si wafer. The film is then heavily doped with phosphorus.

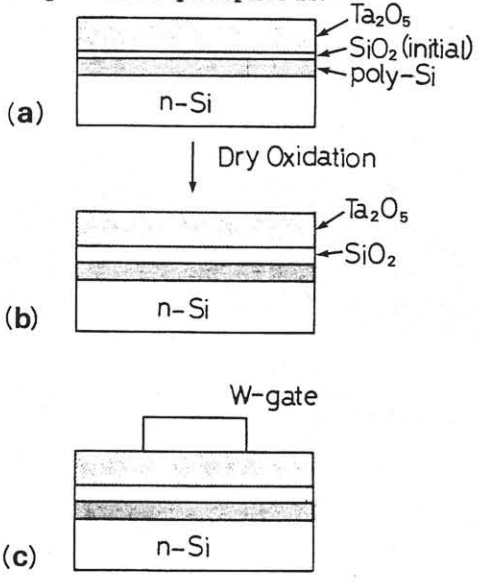

Fig. 1 Fabrication process of W-gate/Ta_2O_5/SiO_2/ poly-Si capacitor.

Next, amorphous Ta_2O_5 films ranging in thickness from 2nm to 20nm are deposited by reactive RF sputtering using an Ar/O_2 mixture. At the beginning of Ta_2O_5 deposition, the surface of the poly-Si is exposed to Ar/O_2 plasma, and extremely thin SiO_2 film is grown on the poly-Si film (4). In (b), annealing is performed at high temperature (800, 850, 900, 950, or 1000℃) in dry oxygen in order to ensure complete oxidation and induce SiO_2 growth at the Ta_2O_5/poly Si interface. In (c), W film for the upper electrode is finally deposited after these dielectrics are formed.

SiO_2 GROWTH AT Ta_2O_5/POLY Si INTERFACE

Fig. 2a and 2b show the cross sectional transmission electron micrograph (TEM) of the Ta_2O_5(7.5nm)/SiO_2 films and Ta_2O_5(3nm)/SiO_2 films on poly-Si respectively, which were oxidized in dry oxygen at 850℃. An increment is observed in the bottom SiO_2 and the bottom layer is estimated to be 2.5nm at the Ta_2O_5(7.5nm)/poly-Si interface in (a), and 4nm at the Ta_2O_5(4nm)/poly-Si interface in (b). This result shows that the increment in SiO_2 at the interface between Ta_2O_5 and poly-Si, as well as at the interface between Ta_2O_5 and single crystal Si (cry-Si)(5), depends on the thickness of the Ta_2O_5 film.

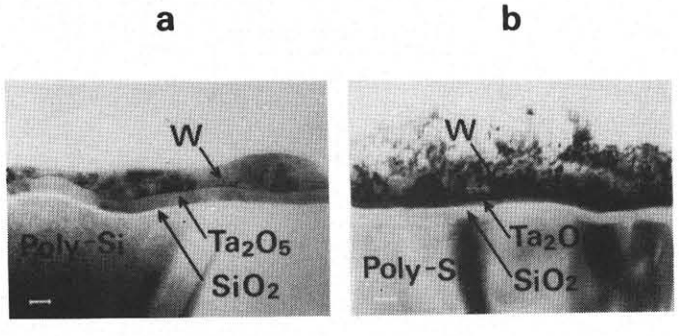

Fig. 2 Cross sectional TEM image of Ta_2O_5/SiO_2 films (scale is 10nm) (a)Ta_2O_5(7.5nm)/ SiO_2 after dry O_2 at 850℃ for 30 mins. (b) Ta_2O_5(3nm)/SiO_2 after dry O_2 at 850℃ for 30 mins.

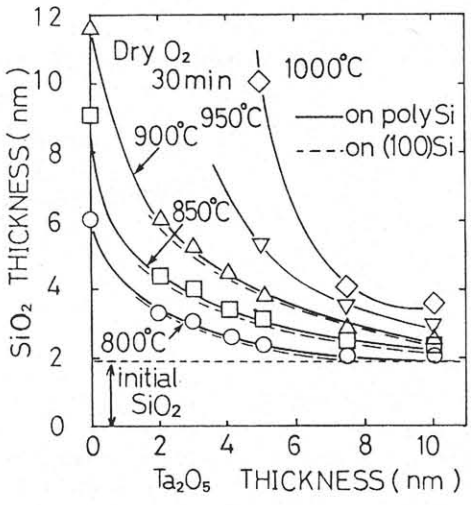

Fig. 3 SiO_2 thickness at Ta_2O_5/poly Si interface after dry oxidation as a function of Ta_2O_5 thickness with annealing temperature as a parameter.

Fig. 3 shows the influence of Ta_2O_5 thickness on SiO_2 growth at the Ta_2O_5 /poly-Si interface and at the Ta_2O_5 /cry-Si interface, with annealing temperature as a parameter. The thickness of the bottom SiO_2 is evaluated by the change in capacitance before and after annealing. As is clear from the figure, as the thickness of the Ta_2O_5 film decreases, the thickness of the bottom SiO_2 formed thereunder increase rapidly. This suggests that the growth mechanism of the bottom SiO_2 can be regarded as diffusion controlled growth, of which the diffusion coefficient is that of the oxydant in Ta_2O_5 film.

DEFECT DENSITY REDUCTION

Fig. 4 shows the defect density of double dielectric films on poly-Si, comparing with thermally grown SiO_2 on cry-Si and on poly-Si. In this paper, the effective film thickness(ts) and effective

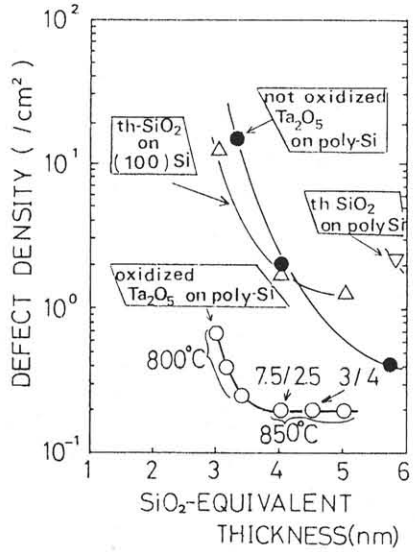

Fig. 4 Defect density of Ta_2O_5/SiO_2 films compared with that of SiO_2 on poly-Si and on single silicon.

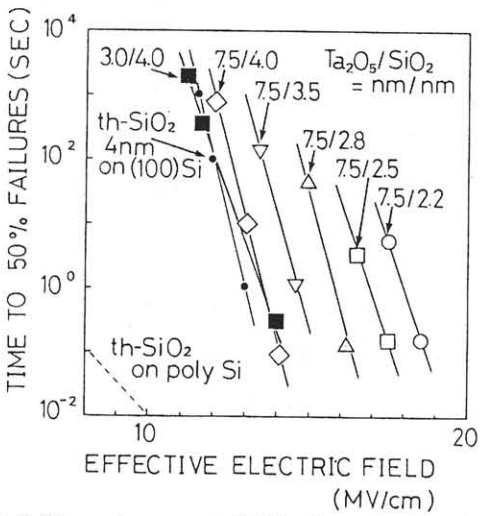

Fig. 5 Dependence of TDDB characteristics on SiO_2 thickness at Ta_2O_5/SiO_2 interface compared with SiO_2 on single Si and on poly-Si.

field(Es) were calculated using a dielectric constant of 3.82 for SiO_2. Dry oxidation reduces the defect densities of the double dielectric films to less than 0.2/cm², from 100 /cm² . This defect density of the double dielectric films is one tenth as large as that of thermally grown SiO_2 on cry-Si and is far less than that for the thermally grown SiO_2 on poly-Si in the region of 4~5nm effective film thickness. One of the reasons for such a low defect density is that at weakspots where the Ta_2O_5 thickness is locally thin, the bottom SiO_2 thickness selectively increases on poly-Si as well as on cry-Si(5).

TDDB CHARACTERISTICS

Fig. 5 shows the results of the time dependent dielectric breakdown (TDDB) characteristics extrapolated to the long term reliability of Ta_2O_5/SiO_2 double dielectric films on poly-Si. Fig. 5 shows that electric field dependence of the time to 50% failure for Ta_2O_5(7.5nm)/SiO_2(2~4nm) double dielectric films on poly-Si, with the bottom SiO_2 thickness as a parameter, compared with thermally grown SiO_2(4nm) on cry-Si. As can be seen in Fig. 5, the time to 50% failure increases as the thickness of the bottom SiO_2 decreases for the same electric field and as the thickness of the bottom SiO_2 reaches 4nm, the time to failure of the films become the same as that of 4nm thermally grown SiO_2 on cry-Si. Ta_2O_5(3nm)/SiO_2(4nm) double dielectric films on poly-Si also exhibit TDDB characteristics similar to that of 4nm thermally grown SiO_2 on cry-Si.

These results suggests that the lifetime to breakdown of the double dielectric films is controlled by the lifetime of the bottom SiO_2. In a recent investigation of the TDDB characteristics of extremely thin thermally grown SiO_2 on cry-Si(6), it was clarified that as the thickness of SiO_2 on cry-Si was reduced to less than 5nm, the lifetime to breakdown greatly increased. Accordingly, by setting the thickness of the bottom SiO_2 film to be thinner within practical limit for defect density, highly reliable dielectric film can be obtained. When the thickness of the bottom SiO_2 is fixed at about 2nm, the lifetime to breakdown of double dielectric film is more than 4 decades longer than that

of thermally grown SiO_2 on cry-Si in the 4~5nm effective film thickness region.

CONDUCTION PROPERTIES

Fig. 6 shows the J-E characteristics of the double dielectric films in which the thickness of the bottom SiO_2 is fixed at about 2nm, and the effective film thickness is 3, 4 and 5nm. These J-E characteristics are compared with thermally grown 3, 4, and 5nm SiO_2 on cry-Si and the thermally grown 6nm SiO_2 on poly-Si. This figure shows that even in the 4~5nm effective film thickness region, a leakage current of $10^{-8}A/cm^2$ can be obtained at 5MV/cm, of which current is as same as the leakage current of the double dielectric films formed on cry-Si. These results suggest that the quality of the bottom SiO_2 on poly-Si is not inferior to the bottom SiO_2 on formed on cry-Si. As is well known, the thickness of thermally grown oxide on poly-Si varies considerably over the wafer surface due to the difference in the growth rate of the various crystal faces. However, the bottom SiO_2 in

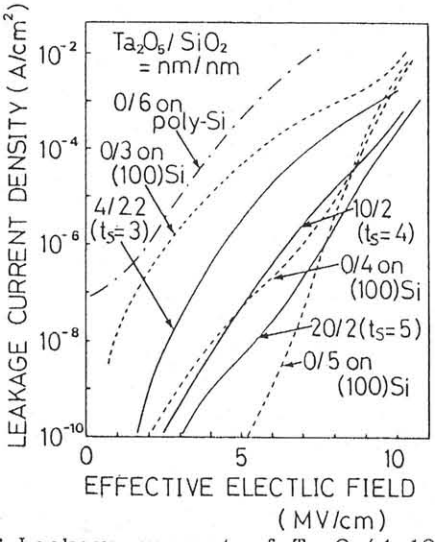

Fig. 6 Leakage current of Ta_2O_5 (4, 10, and 20nm) /SiO_2 capacitor after 800℃ dry oxidation for 30 mins, having effective film thicknesses of 3, 4 and 5nm, are compared with SiO_2 (3, 4 and 5nm) on single crystal Si and poly-oxide(6nm).

Ta_2O_5/SiO_2 system is grown with diffusion controlled oxidation, as mentioned before, so that local variations of growth rate seem to be lost and uniform oxidation occurs. This uniform oxidation inhibits the generation of asperities.

CONCLUSION

In the region of 4~5nm effective film thickness, Ta_2O_5/SiO_2 double dielectric films are shown to have low defect density, sufficient TDDB reliability and low leakage current. This double dielectric films with thinner bottom SiO_2 is more resistant to breakdown. These films with about 2nm bottom SiO_2, of which the effective film thickness is 4~5nm, have more than 4 decades longer lifetime to breakdown than thermally grown SiO_2 on single crystalline Si and have a leakage current of less than $10^{-8}A/cm^2$ at 5MV/cm.

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