Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 243-246

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Characteristics of Si Epitaxial Layers Grown by a New RF-Induction Heated Hot-Wall Type Reactor for High Volume, Low Cost Epitaxy

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Silicon epitaxial layers grown by a newly developed RF-induction heated hot-wall type reactor (prototype), which is capable of processing 10-20 5-inch diameter wafers per 100 mm of stack length, have been characterized. Satisfactory uniform layers with low undoped donor concentration ($\sim 5\times10^{13}$ cm^{-3}) and high crystalline quality could be obtained. The p^+-n(epi)-n^+ junction diodes exhibited almost ideal breakdown and reverse leakage characteristics. The C-t response and the quasi-static C-V measurements from Al gate MOS capacitors showed high minority carrier generation lifetimes of 150-800 μs and interface trap level density comparable to that of bulk CZ silicon, respectively. An undesirable effect from HCl addition to the growth nutrient gas on undoped donor level and carrier lifetime was observed.

1. Introduction

A new growth reactor which can provide high volume, low cost silicon epitaxial wafers is required to meet the trend towards increased use of epitaxial wafers in CMOS devices, in addition to the conventionally used bipolar and Bi-CMOS devices. A few studies attempting to achieve high growth throughput have been reported. Ban (1) and Bloem et al. (2) have reported on high capacity reactors in which wafers are parallelly arranged in a stack-like packing manner. However, these reactors have not been put to general use yet. Quite recently, Tetron developed another reactor with high capacity which is achieved by facing near-vertical wafers across from each other in a circular cluster of tapered cavities (3). However, details concerning its performance have not been reported yet.

At first, in this paper, a prototype high-volume epitaxial reactor designed on a new concept is presented briefly. Then the discussion focuses on the obtained characteristcs of the growth layers. Details of the reactor design and uniformity control method of the layer thickness are to be presented elsewhere (4).

2. Experimental

Figure 1 shows a schematic diagram of the RF-induction heated hot-wall type reactor that we designed and constructed. Its main features are as follows:

(i) Substrate wafers are parallelly stacked in the vertical direction on a rotating quartz holder, which enables high volume wafer loading per batch.

(ii) Wafers are RF-induction heated by the surrounding silicon carbide coated graphite hot-wall susceptor.

(iii) Multiple (two in the present experiments) nutrient gas ($SiCl_4$+H_2) distributor tubes are arranged on one side of the wafers. The nutrient gas is injected homogeneously into all the wafer-to-wafer spacings.

(iv) HCl gas is introduced into the nutrient gas in order to prevent silicon deposition on the quartz parts in the reactor.

This reactor is capable of processing at least 10 wafers (5 inch dia.) per 100 mm of stack length. Moreover, if wafers are hold in a back-to-back manner, growth of 20 wafers per 100 mm of stack length becomes possible. This amounts to at least 50-100 wafers per batch, if a holder of 500 mm stack length is used.

The substrates used for experiments were with the ⟨100⟩ surface direction, Sb donor impurity and

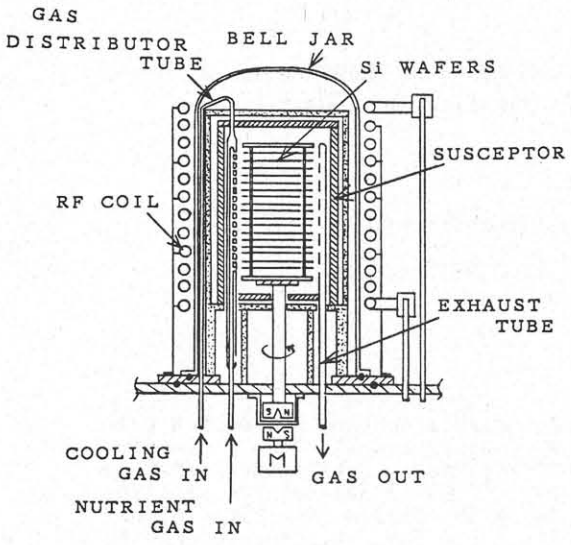


Fig. 1. Schematic representation of RF-inducdtion hot-wall epitaxial reactor.

0.015 ohm-cm resistivity. The substrates were pre-heated for 20 min at 1060-1110 ℃ in H_2. Then, undoped or phosphorous doped epitaxial layers of 10-15 μm thickness were grown at 1060-1110 ℃ with growth rates of 0.2-0.3 μm/min. Two kinds of epilayers were prepared by supplying nutrient gas with and without adding HCl gas in order to compare the layer characteristics.

Crystalline defects of the grown layer were examined by the Wright etching method. Electrical characteristics were evaluated by using p-n junction diodes and MOS structure diodes. Junction diodes of 1.1 mm diameter with a mesa-type structure were made by boron diffusion into the epilayer at 1100 ℃ for 20 min using a BN source. The silicon oxide layer (110 nm thick) of the MOS diode was formed at 1000 ℃ in pyrogenic steam. Aluminum was deposited by E-B evaporation and patterned to make electrodes of 1.0 mm diameter on the oxide layer. The MOS diodes were annealed at 500 ℃ for 30 min in H_2 before C-V and C-t characteristics measurements.

3. Results and discussion

Figure 2 shows a typical example of the thickness distribution (i.e., growth rate distribution) within a wafer. Uniform distribution of ±3% can be achieved by choosing optimum gas flow conditions for the two gas distributor tubes. Typical results of the growth rate variation along the direction of the wafer stack are shown in Figure 3. Uniform distribution with less than ±5% deviation is obtained between the stack length of about 180-200 mm. This allows loading of about 20 wafers and if wafers are laid in a back-to-back manner, about 40 wafers per batch can be loaded with thickness variations of less than ±5% both within a wafer and between wafer-to-wafer. In these cases, the resistivity variations both within a wafer and between wafer-to-wafer are less than ±10%.

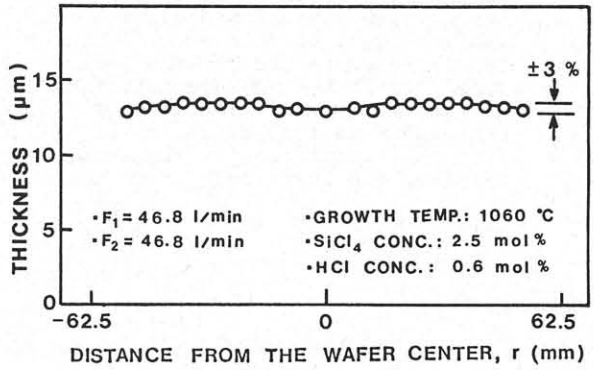


Fig. 2. A typical example of the thickness distribution (i.e., growth rate distribution) within a wafer.

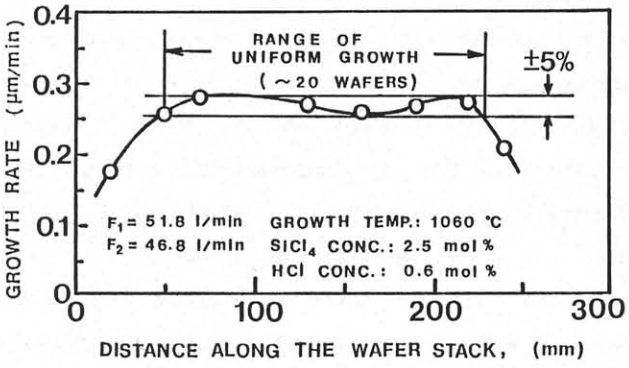
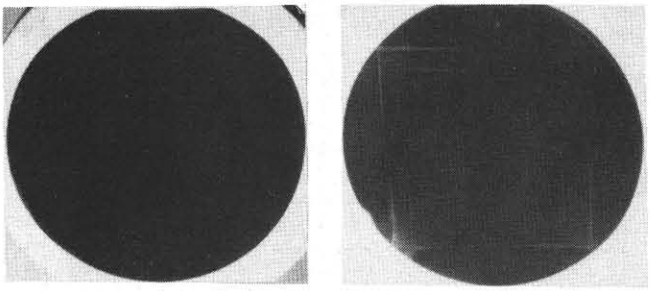


Fig. 3. Growth rate distribution along the direction of the wafer stack.

Then the crystalline quality was examined by the defect delineation etching method. Figure 4 indicates two examples, where (a) used a quartz wafer holder (type A) in which each wafer was placed on three pawls protruding from three props and (b) used a quartz holder (type B) in which each wafer was supported by three grooves notched on three props. In the latter, slip lines generated from the points corresponding to the grooves of the

holder can be seen. By optimizing the configuration of the wafer holder, epitaxial wafers with neither slip lines nor other defects such as stacking faults and dislocations can be obtained.



(a) (b)

Fig. 4. Photographs of the wafer surface after defect delineation etching for (a) type A wafer holder and (b) type B wafer holder.

One of the features of this growth method is adding HCl gas to the nutrient gas. Therefore we investigated the layer characteristics, paying attention to the effects of HCl addition.

Figures 5 (a) and (b) show the donor concentration profiles of the epitaxial layers grown with and without adding HCl to the nutrient gas, respectively, which were measured by the C-V method. These epilayers were grown without any intentional donor impurity doping. Low donor concentration levels (i.e., high purity levels) of about 5×10^{13} cm^{-3} ($\sim$100 ohm-cm) are obtained in both cases. However, the donor concentration level of the HCl added epilayer is somewhat higher than that of the no HCl added epilayer. The dopant (Sb donor) transition region widths at the donor concentration level of 1×10^{15} cm^{-3} for both growth layers are about the same, i.e. 0.7 μm, indicating that the introduction of HCl has almost no influence on the autodoping effect.

The V-I characteristics of typical p-n junction diodes are shown in Figures 6 (a) and (b). Breakdown voltages of 70~150 V for the various epilayer thickness between 1.5-10 μm are obtained, which coincide fairly well with the theoritical values. Figure 6 (b) exhibits almost ideal reverse leakage characteristics. These results demonstrate that the growth layer is of superior quality.

Figures 7 (a), (b) and (c) show the interface trap level density (D_{it}) distribution of an Al gate

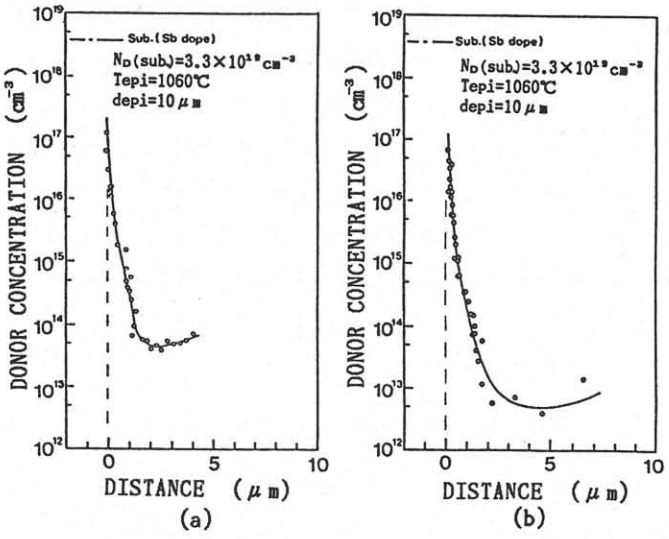
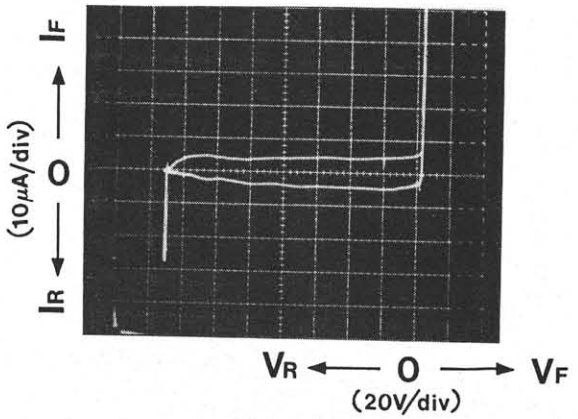
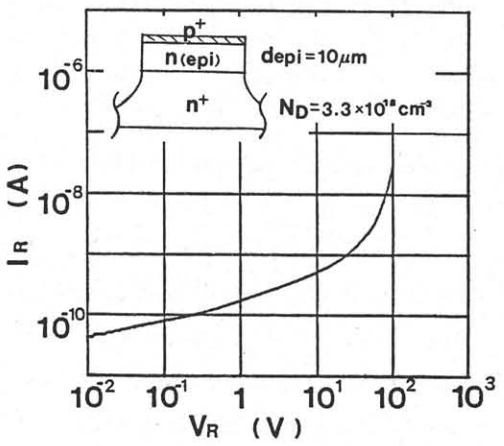


Fig. 5. Donor concentration profiles in the undoped epitaxial layers (a) deposited with added HCl gas and (b) deposited without added HCl gas.



(a)



(b)

Fig. 6. Typical I-V characteristics of epitaxial p-n junction diode, (a) I-V characteristics measured by curve tracer and (b) reverse leakage characteristics.

capacitor fabricated by using various crystal materials, which were obtained by quasi-static C-V curves. The interface trap density at midgap for the sample fabricated on the epitaxial layer grown by adding HCl gas was less than 10^{11} $cm^{-2}eV^{-1}$ and comparable to those for samples fabricated on the epitaxial layer grown without added HCl gas and on the bulk CZ silicon.

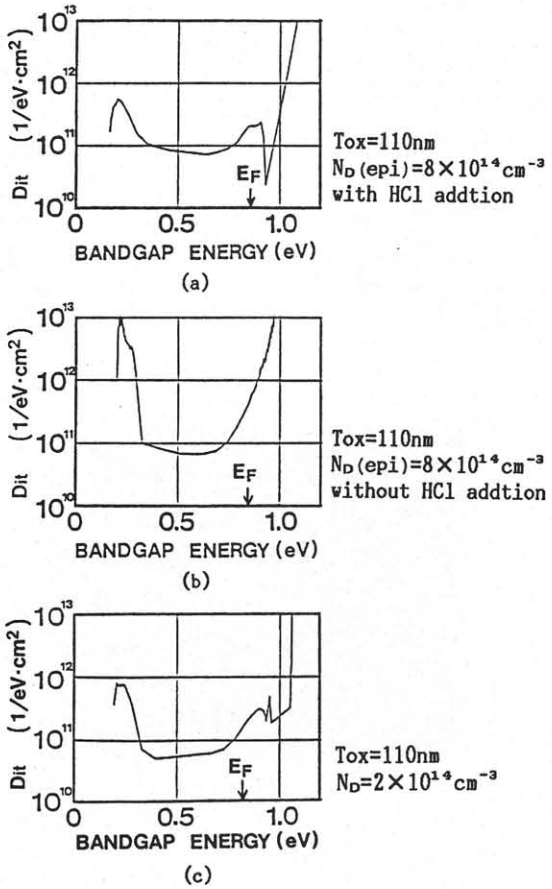


Fig. 7. Interface trap level density, (D_{it}) distribution at Si-SiO_2 for (a) epilayer grown with added HCl gas, (b) epilayer grown without added HCl gas and (c) bulk CZ silicon.

The minority carrier generation lifetime of the epitaxial layer grown by this new reactor was measured using the C-t response method and compared with that of the bulk CZ silicon (Figure 8). Relatively long lifetime can be obtained even if no intentional gettering process is applied, although the lifetime of the epitaxial layer grown with HCl addition is somewhat lower than those of the epitaxial layer grown without HCl addition and of bulk CZ silicon. This lowering of the lifetime would be eliminated by using a higher purity HCl addition system.

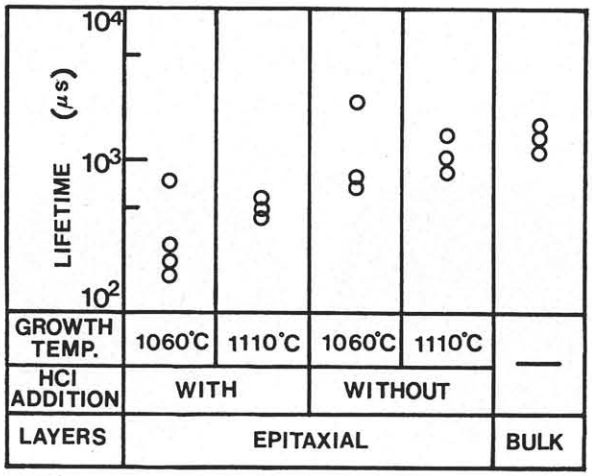


Fig. 8. Minority carrier generation lifetimes of various epilayers and bulk CZ silicon.

4. Conclusion

We have designed and constructed a new epitaxy (prototype) reactor capable of processing a high volume of wafers. Satisfactory thickness and resistivity uniformity as well as electric charactristics could be obtained. Now longer lifetimes are desired by adopting a higher purity HCl addition system.

ACKNOWLEDGMENTS

We wish to express our sincere thanks to Dr. M. Okamura, K. Miyata, M. Ohta and M. Fujita for their guidance and encouragement in this work. We also would like to thank M. Akiyama for his assistance in the experimental work and M. Ohue and H. Onose for their helpful discussions.

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