Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 263-266

GaAs MESFETs Fabricated by New Self-Alignment Technology

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Newly developed self-alignment technology is applied to high frequency GaAs MESFETs. This new technology uses the selective etching of different insulators to fabricate fine gates less than a quarter micron. Furthermore, a double recess structure and a offset gate structure are realized at the same time in the self-alignment method, so that high gain and high breakedown voltage are obtained. At 28GHz, the 0.2μm gate MESFET exhibited a linear gain of 4.2dB and an output power of 0.31W/mm, thus demonstrating the effectiveness of the new technology.

1 Introduction

Solid state analog devices operating at high frequency have been studied as key devices for advanced communication system. GaAs MESFETs applied in this field must satisfy several requirements such as high operating voltage (i.e. high breakdown voltage) and high gain at the same time. In order to achieve high gain, it is necessary to realize very fine gates. Electron Beam lithography, Focused Ion Beam lithography and some specialized selective ething technologies have been developed to achieve a quarter micron gate. On the other hand, breakdown voltage have been improved by employing an offset gate structure [1] in which the gate is placed not at the center of source-to-drain region, but nearer to the source. The offset gate structure, however, usually reduces the transconductance gm of MESFETs and results in poorer gain at high frequency.

In order to resolve the above problem, new device structure and new self-alignment technology are proposed and descrived in this paper. Characteristics of 0.2μm gate MESFETs are also shown.

2 New Self-Alignment Technology

A Device Structure

Cross section of the GaAs MESFETs fabricated by the new self-alignment technology is shown in Fig. 1. The source-to-gate region is single recessed and the gate-to-drain region is double-recessed. Furthermore, the gate has a T-shaped cross section, and is offset nearer to the source. This structure has the following features; First, source-to-gate resistance is reduced because of the smaller distance. Second, the influence of surface potential [2] which causes a so called long-gate effect is

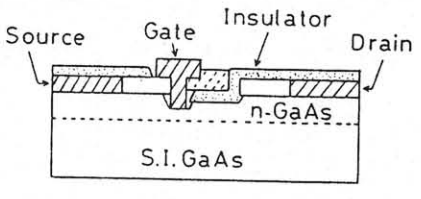

Fig. 1 Cross section of the proposed GaAs MESFET.

eliminated, so that high transconductance gm or high gain can be achieved. Third, the T-shaped gate contributes to lowering the gate resistance, therefore resulting in higher gain. Fourth, the offset gate structure is effective in improving breakdown voltage. Some of those features will be discussed later.

B Fabrication Process

The consecutive process steps which constitute the new self-alignment technology are summarized in Fig. 2(a) to (f); the detailes are described below.

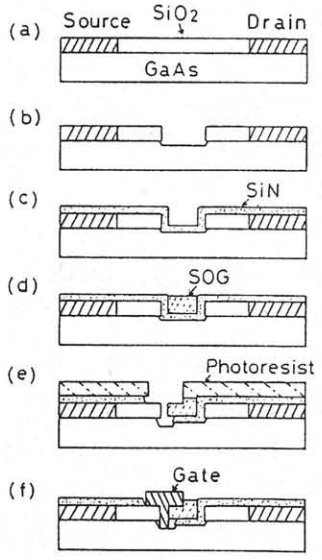

Fig. 2 Schematic fabrication steps in the new self-alignment technology.

First, SiO_2 is deposited on a GaAs substrate which has a thin active layer. This is followed by the formation of source and drain electrodes as shown in Fig. 2(a). SiO_2 is ethed in the source-to-drain region, while the GaAs active layer is ethed only slightly (1st recess ething) as shown in Fig. 2(b). SiN is deposited as shown in Fig. 2(c). SOG (Spun-On-Glass) is coated by a spinner followed by an etch back process, and the groove is filled with SOG, as shown in Fig. 2(d). The surface is then covered with photoresist except for the area which includes the SiN sidewall nearer to source. After SiN is selectively and almost vertically ethed by using RIE (Reactive Ion Ething), the active layer is ethed (2nd recess etching) as shown in Fig. 2(e). Gate metal is evaporated and lifted off, and the MESFET is completed as shown in Fig. 2(f).

Here the following should be noted; First, gate length is determined by the thickness of SiN deposited in step (c). Second, the appearance of the double recess is asymmetrical, i.e. a deep single recess on the source side, and a shallow double recess on the drain side. Third, the offset gate and double recess structure are formed using a completely self-alignment method.

3 Results and Discussions

A Fine Gate Feasibility

As described previously, gate length is controlled by the thickness of the deposited SiN in this new technology. SiN thickness Tsi_N versus attained gate length Lg is plotted in Fig. 3. Gate length from 0.34 μm to 0.16 μm were achieved with SiN thickness from 0.55 μm to 0.30 μm. It is also seen that the ratio of attained gate length to

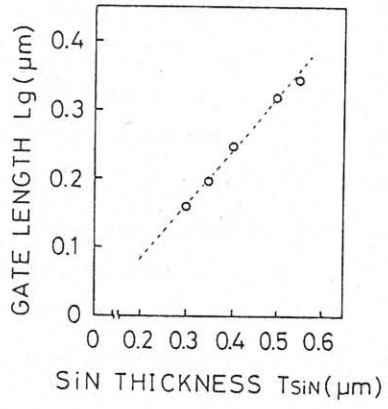

Fig. 3 Gate length Lg versus SiN thickness Tsi_N.

deposited SiN thickness was about 0.6 and always constant. This means that less than a half micron gate can be realized with good controllability. By extraporating the experimental results, it can be seen that a gate length less than 0.1 μm is realized with SiN thickness of less than 0.2 μm.

Here the ratio 0.6 results from the fact that SiN thickness on the SiO_2 sidewall is thinner than on other areas by a ratio 0.6. This is seen in Fig. 4. The reason for this, however, is not yet clear.

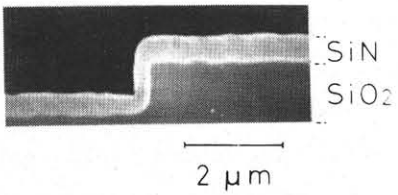

Fig. 4 Cross section of SiN film deposited at SiO_2 step.

B Effects of Double Recess Structure

The effects of introducing a double recess structure is discussed below. Transconductance gm and drain breakdown voltage BVd in the two different devices, i.e. one in double recess structure and the other in single recess were compared.

Fig. 5 showes the results when gate-to-drain distance Lgd was varied, where the width of the first recess was held constant and carrier concentration was $2.0 \times 10^{17} cm^{-3}$. Both types of devices have considerably higher drain breakdown voltage. On the other hand, the gm of the double recess structure is one and a half times larger and does not decrease as much with larger Lgd compared with the single recess structure.

Thus, it can be concluded that the double recess structure realizes high transconductance as well as good drain breakdown voltage.

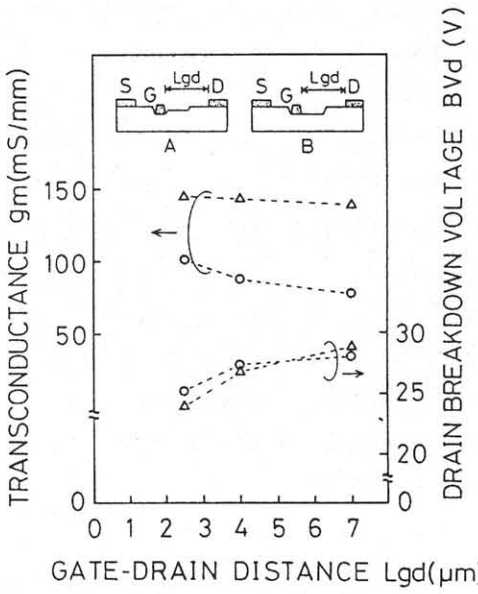

Fig. 5 Transconductance gm and drain breakdown voltage BVd versus gate-drain distance Lgd. △ and ○ correspond to device structure A and B respectively.

The reason the double recess structure showes higher gm was also analyzed by device simulation using a 2-D simulator CANNON [3]. Electric field distribution in the channel region between the gate edge and the drain edge was calculated, and the results are shown in Fig. 6. When the gate is fabricated using a 0.1 μm recess, the strongest electric

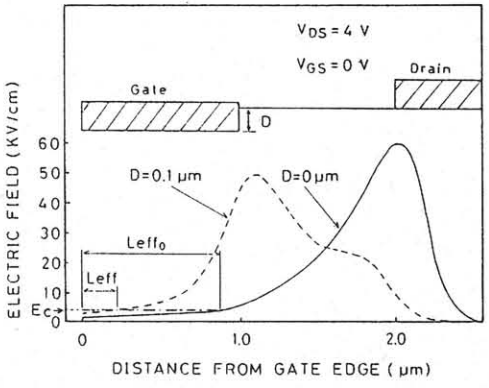

Fig. 6 Electric field in channel. D stands for recessed depth. Leff and $Leff_0$ are effective gate length when D=0.1 μm and 0 μm respectively. Ec is critical electric field at which electrons reach saturation velocity.

field exists near the gate edge. On the other hand, when the gate is fabricated without the recess (i. e. planner structure), the position of the strongest field moves to the drain edge. Since the effective gate length (indicated by Leff and Leff $_0$) is defined by the constant mobility region, Leff $_0$ in the planner structure is larger (long-gate effect) than Leff in the recess structure. Thus, the recess structure can avoid gm degradation caused by the above long-gate effect.

C Characteristics of GaAs MESFETs

A cross sectional SEM photograph of a GaAs MESFET fabricated by the new self-alignment technology is shown in Fig. 7. It can be seen that the gate is offset, that

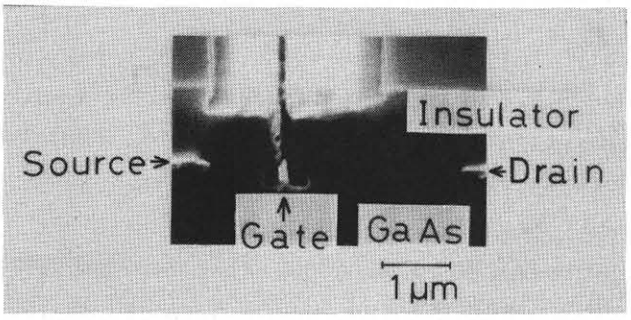

Fig. 7 Cross sectional SEM photograph of the MESFET.

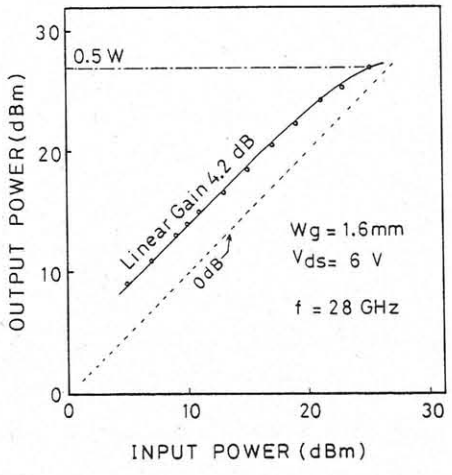

Fig. 8 Input-output characteristics of the MESFET.

the gate-to-drain region is double-recessed, and that a 0. 2 μm T-shaped gate is realized.

The input-output power characteristics of the GaAs MESFET having 1. 6mm gate width was measured at 28GHz and the results are shown in Fig. 8. A linear gain of 4. 2dB and an output power of 0. 5W (0. 31W/mm) at 1dB compression point were obtained.

These characteristics demonstrate effectiveness of the new technology.

4 Conclusion

A new self-alignment technology has been developed for high frequency GaAs MESFETs. With this technology, a offset gate and double recess structure were fabricated using the self-alignment method. Furthermore, very fine gate less than a quarter micron could be realized even by conventional light lithography. At 28 GHz, the 0. 2 μm gate GaAs MESFET operating under large signal conditions obtained a linear gain of 4. 2dB and an output power of 0. 5W (0. 31W/mm), thus demonstrating the effectiveness of the new technology.

Acknowledgement

The authors wish to thank Dr. K. Hiruma and all the members of the MBE-Group for performing epitaxial layer growth and K. Sekine for making the r. f. measurements. Thanks are also due to Dr. H. yanazawa and Dr. M. Miyazaki for their constant support throughout this work.

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