Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 267-270

High Speed Inverted-HEMT Logic with a Sub-Half-Micron Gate

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A short gate length inverted HEMT using a new gate fabrication technique is reported. In the technique, the photoresist opening for gate formation was narrowed by evaporated Ti at a small angle. By using this technique, not only the gate length was reduced but also the Schottky characteristics were improved. The uniformity of threshold voltage was not degraded. A 0.28μm gate I-HEMT was fabricated and the small drain conductance of 13mS/mm was observed. The minimum propagation delay time of 11.9psec/gate with a power dissipation of 0.560mW/gate was obtained for a 0.5μm gate DCFL ring oscillator at room temperature.

1. Introduction

The selectively doped GaAs/n-AlGaAs single heterostructure has been used widely for high speed IC's.[1-3] But in these reports the heterostructure of a ternary on top of a binary (conventional HEMT) was used because of the difficulty in the growth of inverted heterostructure. In the inverted HEMT (I-HEMT), the source resistance can be easily lowered by the top n^+-GaAs layer, therefore the high performance is expected at room temperature. We already reported a growth condition for inverted heterostructure and an I-HEMT with high transconductance (400mS/mm) at room temperature.[4] Moreover, I-HEMT has a small short channel effect because 2-dimensional electron gas(2-DEG) is confined by the back AlGaAs layer. In this paper we report a short gate length I-HEMT using a new gate fabrication technique.

2. Crystal Growth and Device Fabrication

The inverted heterostructure was grown by conventional III-V MBE system. A 2-inch HB semi-insulating GaAs substrate was used as a substrate. A schematic cross section of an inverted HEMT is shown in Figure 1. An epitaxial layer consists of undoped GaAs and AlGaAs(both 1000Å), n-AlGaAs($1.1\times10^{18}cm^{-3}$, 80Å), undoped AlGaAs(40Å), undoped GaAs(200Å), n-GaAs($5\times10^{17}cm^{-3}$, 500Å), and n^+-

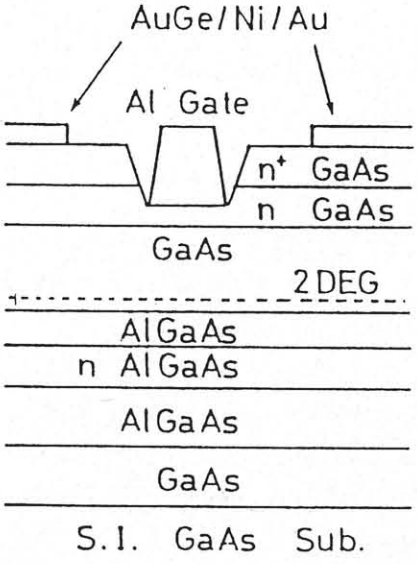


Fig.1 Schematic cross section of an I-HEMT.

GaAs($4\times10^{18}cm^{-3}$, 500Å). The maximum carrier concentration of 2-DEG is $9\times10^{11}cm^{-2}$. The I-HEMT was fabricated as follows. First, devices were isolated by ion implantation of oxygen to form a planar structure. Source and drain contacts were formed by the AuGe/Ni/Au system. The gate was formed using a new technique(angle evaporation technique) which is shown in Figure 2. (a) a 0.6μm thick LMR photoresist[5] as a gate etching mask was developed by a deep-UV contact lithography. Gate regions were recessed by 50eV Ar ion-beam. The threshold voltages were controlled by the recessed depth. (b)Next, Ti was evaporated at a small incident angle onto both sides of the mask walls. (c) Al metal was evaporated and consequently a self-aligned gate was patterned by liftoff. By this new technique, not only a gate length was reduced but also a gate was effectively separated from an n^+-GaAs layer about 0.1μm. Figure 3 shows a SEM photograph of an FET cross section after gate metal(Al) evaporation. 1000Å thick Ti layers can be seen on both mask walls. No Ti contamination is observed in the recessed region. In the photograph, the gate length is shortened to 0.3μm with photoresist opening of 0.5μm.

3. Schottky Characteristics

By employing the angle evaporation technique, gate was formed apart from an n^+-GaAs layer, and hence Schottky characteristics were improved. Figure 4 shows Schottky characteristics without (a) and with (b) Ti angle evaporation. $0.5\times10\mu m^2$ Schottky gates were used for measurements. The Schottky built-in voltage and the breakdown voltage at the gate current of ±10uA were improved from 0.45V and 4.4V to 0.53V and 8.8V, respectively. This gate fabrication technique is useful for improvement of Schottky characteristics as well as reducing a gate length.

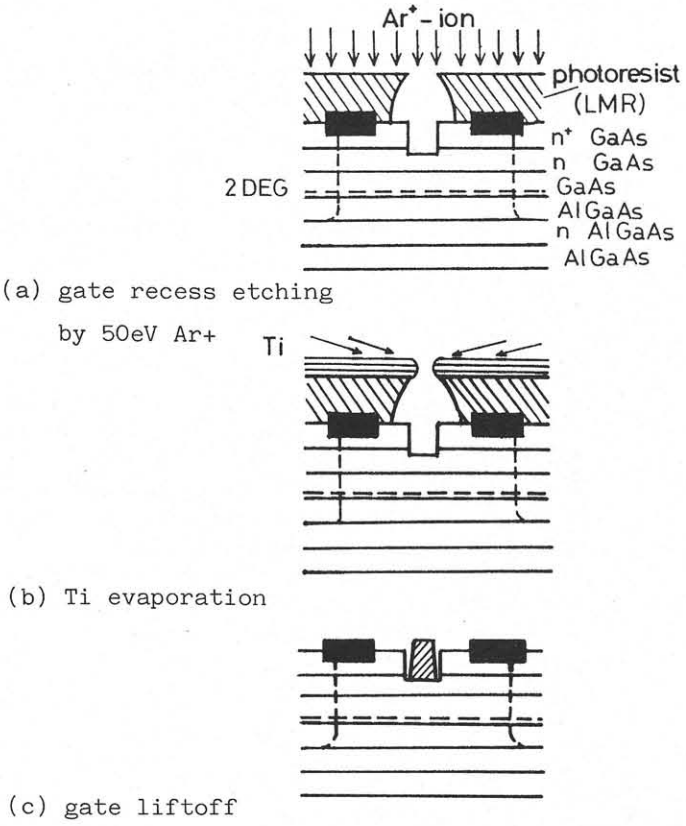


Fig.2 Gate fabrication process flow.

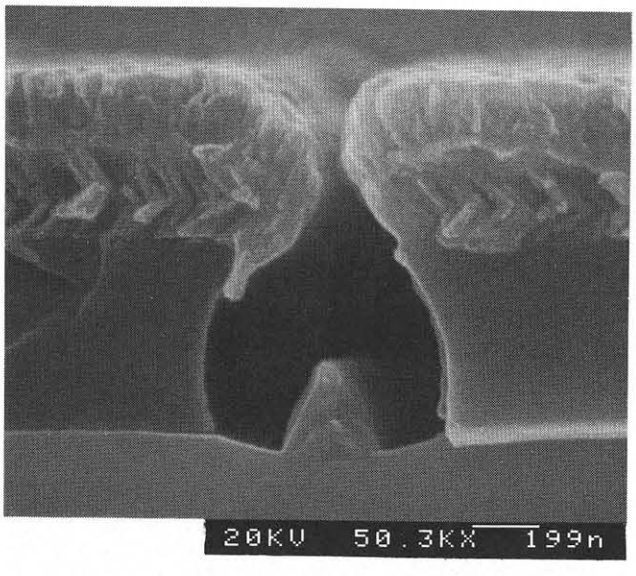


Fig.3 A SEM photograph of a cross section of I-HEMT after gate metal evaporation.

4. Threshold Voltage Uniformity

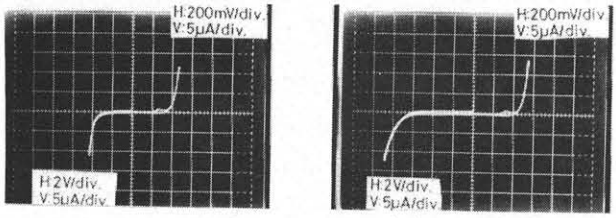
To fabricate LSI, the threshold voltages have to be uniform on a microscopic as well as a macroscopic scale. We evaluated the microscopic uniformity using 50μmx50μm pitch FET arrays.[6] Figure 5 shows the distributions of threshold voltages of 0.5 μm gate I-HEMT's(enhancement mode FET:E-FET and depletion mode FET:D-FET). The standard deviations of Vth(σVth) were 11mV at the mean Vth($\overline{Vth}$) of 61mV, and 43mV at $\overline{Vth}$=-637mV. The macroscopic uniformity in a 2-inch wafer was measured on the same one. The σVth was 27.6mV at $\overline{Vth}$=84mV. These results show the uniformity of Vth is not degraded by this new technique and is sufficiently small to fabricate LSI.

5. Characteristics of Quarter-Micron I-HEMT

By employing the angle evaporation technique, an I-HEMT with a sub-half-micron gate length was fabricated. Figure 6 shows the I-V characteristics of a 0.28μm gate length I-HEMT. Saturation characteristics of drain current is fairly good, showing the small short channel effect. The drain conductance of I-HEMT is shown in Figure 7 as a function of gate length. The small drain conductance of 13mS/mm was obtained at the gate length of 0.28μm. This result shows that a 2-DEG is tightly confined by a hetero-barrier in an I-HEMT.

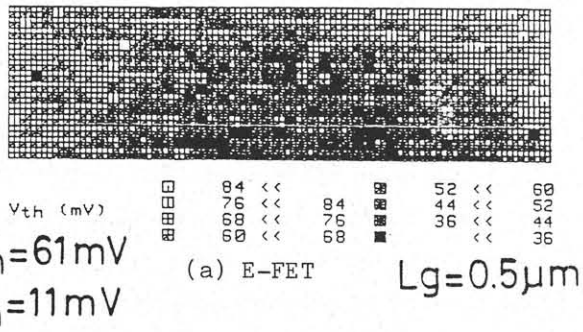
6. Ring Oscillator

The propagation delay of E/D type DCFL gate was measured at room temperature using a 21-stage ring oscillator. The dependence of the propagation delay and the power dissipation on the supply voltage is plotted in Figure 8. The power dissipation depends linearly on the supply voltage, and the propagation delay is almost constant. No dependence of the propagation delay on the power dissipation may be due to the good saturation charateristics of drain current. When the supply voltage is lower than 2 V,



(a) Without Ti evaporation (b) With Ti evaporation

Fig.4 Schottky characteristics of I-HEMT's.



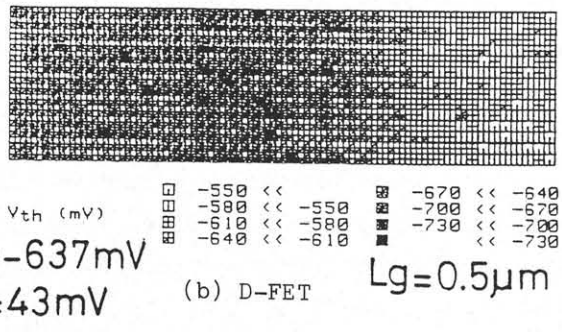


Fig.5 Vth distributions of I-HEMT's using 50μmx50μm pitch FET arrays.

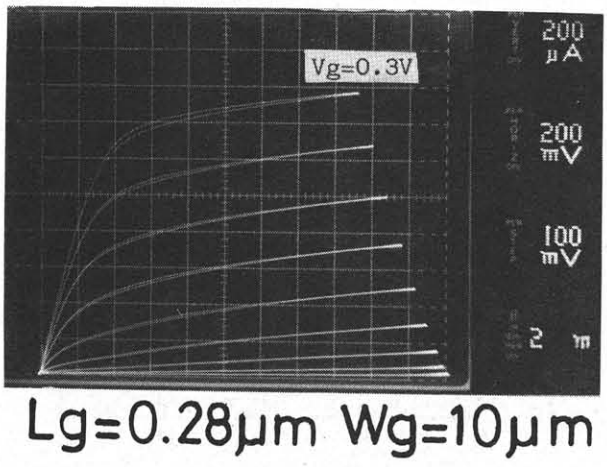


Fig.6 I-V characteristics of 0.28μm gate length I-HEMT.

the propagation delay is a little decreased due to the decrease of the logic swing. The fastest switching speed at room temperature was 11.9psec/gate with a power dissipation of 0.560mW/gate at a supply voltage of 0.59V.

7. Summary

We have demonstrated a short gate length I-HEMT using a new gate fabrication technique. The microscopic uniformity was studied using the 50μmx50μm pitch FET arrays. The standard deviation of 11mV at Vth=61mV was obtained with the 0.5μm gate length, which was sufficiently small to fabricate LSI. The drain conductance of 0.28μm gate I-HEMT was 13mS/mm indicating a very small short channel effect. The minimum propagation delay of a DCFL gate with 0.5μm I-HEMT's was 11.9psec/gate with the power dissipation of 0.560mW/gate. These results confirmed that an I-HEMT with even a sub-half-micron gate is suitable for high speed LSI's.

8. Acknowledgement

The present research effort is part of the National Research and Development program on "Scientific Computing System", conducted under a program set by the Agency of Industrial Science and Technology, Ministry of International Trade and Industry.

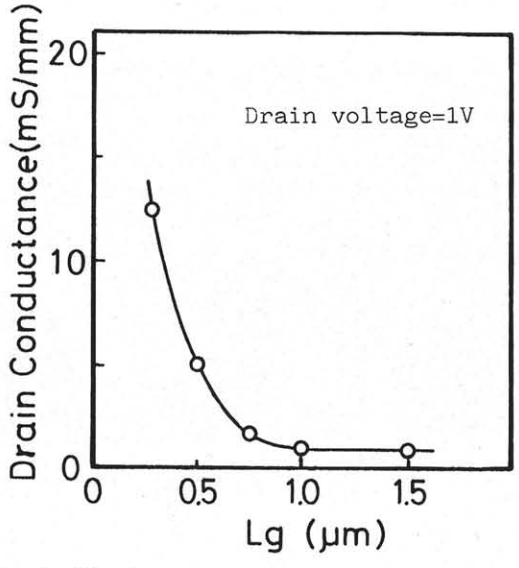


Fig.7 Drain coductance as a function of gate length.

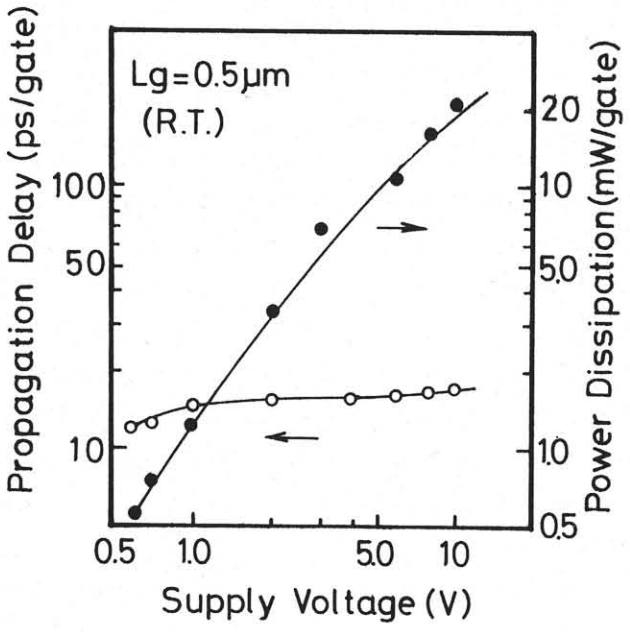


Fig.8 Dependence of propagation delay and power dissipation on supply voltage.

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