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A High Voltage GaAs Power Static Induction Transistor

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Recessed gate GaAs power static induction transistors (SITs) with high blocking voltages are described. The rectangular grooves in the recessed gate regions were formed by utilizing the anisotropic etching properties of GaAs. The sidewall dielectric layer acted as a mask for implanting magnesium in the bottom of the etched grooves, and as a surface passivation for the p-n junction. Devices with blocking voltages of up to 400 V, fabricated by these methods, had the on-resistance of 18 m$\Omega \cdot cm^2$ and the turn-off speed of 20 ns, which are about five times lower and twice as fast, respectively, of silicon power MOSFETs with the same blocking voltages.

1. INTRODUCTION

Ideal power devices should have characteristics of a low forward voltage drop, a high switching speed, and a low gate drive power. Silicon power MOSFETs offer a short turn-off time due to the absence of minority carrier-storage during operation and low input power for the insulated gate structure, as well as a large ASO due to the negative temperature coefficient of the drain current. However, their on-resistance is several times higher than that of bipolar transistors. It has been calculated[1),2)] that the on-resistance of power devices made from GaAs instead of Si should be at least ten times lower. Static induction transistors (SITs)[3)] are well suited as GaAs power devices, because an inversion layer has not been formed in MOS or MIS structures made from GaAs. But it has not been shown whether GaAs power SITs[4),5)] have lower on-resistance in comparison with silicon devices.

In this paper, GaAs power SITs with a recessed gate feature[6)] and blocking voltages of up to 400 V were fabricated. Low on-resistances and fast switching speeds, which are peculiar to GaAs power devices and have not been obtained in silicon devices, were observed.

2. DEVICE STRUCTURE AND FABRICATION

The recessed gate SIT structure is shown in Fig. 1. This device structure has gate junctions and gate electrodes at the bottom of eched grooves, which are separated from the source in the vertical direction. The gate-to-source breakdown voltages can be controlled by regulating the depth of the grooves without causing a large influence on the drain conductance for the surface gate SIT. The gate resistance of this device with the gate electrode in the each groove is less than that of the buried gate SIT with low hole mobility.

To fabricate the recessed gate SIT, two layers are grown on a (100) oriented and Si-doped GaAs substrate by vapor phase epitaxy. First an n^- layer with a thickness of about 40 μm and a carrier concentration of about $4 \times 10^{13} cm^{-3}$ is grown on the n^+ substrate. The n^+ layer grown on the n^- layer is 0.5 μm thick with a carrier concentration of about $2 \times 10^{18} cm^{-3}$. The epitaxial surface is coated with a 1 μm thick SiN layer, which is then patterned by reactive ion etching (RIE). A 0.5 μm thick layer of PSG is deposited on the surface with treated SiN and etched by RIE again as shown in Fig. 1(a). The edges of the PSG layer, which act as masks for etching GaAs, are set parallel to the $<100>$ directions. The rectangular grooves across the unmasked regions of the GaAs are formed by utilizing the anisotropic etching properties as shown in Fig. 1(b). The etchant is a mixture of NH_4OH, H_2O_2 and H_2O. The same method has been used for forming the termination[7)] of a mesa junction with high blocking voltage between the gate and source. After forming the rectangular grooves, PSG is selectively removed by using buffered hydroflouric acid. Then the wafer is again coated with another

1 μm thick layer of PSG film as shown in Fig. 2(c). RIE is also used to form the PSG sidewalls, which act as the mask for implanting Mg perpendicularly in the bottom of the grooves as shown in Fig. 2(d). After etching PSG and SiN, the wafer is coated with SiO_2 and annealed. PSG/SiN is again deposited as the surface passivation of p-n junction on the surface without an SiO_2 cap. Using RIE, PSG/SiN on the top and bottom of the grooves is removed. AuGe is evaporated perpendicular to the surface. The ohmic contacts are formed by the lift-off method. The AuGe in the gate and source regions is automatically separated by the sidewalls of PSG/SiN. After sintering the contact layers with the AuGe deposited on the backside of the wafer to form the drain, the recessed gate GaAs SIT is complete, as shown in Fig. 3.

3. DEVICE CHARACTERISTICS

Fig. 4 shows the I-V characteristics of the device having structure in Fig. 3. This device had a gate-to-source breakdown voltage of about 70 V. The pentode-like characteristics are obtained at the low gate bias voltages (Fig. 3(a)). The on-resistance in the opening between the gate and source is 18m$\Omega \cdot cm^2$, which is lower than that in shorting (V_{GS}=0 V), because the device with V_{GS}=0 V has a higher channel-resistance due to the reverse-bias potential between the gate and drain caused by the forward voltage drop between the drain and source. When the gate bias is increased in 11 steps of -2 V each, triode-like characteristics are observed as shown in Fig. 4(b). The blocking voltages of 300 V and 400 V are obtained for the reverse gate bias voltages of -30 V and -46.5 V respectively. Fig. 5 shows the on-resistances per unit active area as a function of the breakdown voltage for the GaAs SITs in this study and power MOSFETs. The GaAs SITs have about five times lower on-resistances in comparison with Si MOSFETs with equal breakdown voltages and active areas. Fig. 6 shows typical switching waveforms. Switching speeds as fast as 20 ns are obtained, even faster turn-off speeds can be expected by operating a higher gate bias voltage.[8] Table 1 makes a comparison of the electrical characteristics between the GaAs power SIT and a Si power MOSFET. The GaAs device has about five times lower on-resistance and about twice faster turn-off speed than those of the silicon device.

4. CONCLUSION

The recessed gate GaAs power SITs with blocking voltages of up to 400 V were fabricated by a self-aligned process. A low on-resistance of 18m$\Omega \cdot cm^2$ and a fast turn-off speed of 20 ns, which have not been obtained in Si power devices, were observed.

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REFERENCES

1) B.J.Baliga, J.Appl. Phys. 53(3) (1982) p.1759
2) A.Nakagawa, IEEE ED-33 (1986) p.167
3) J.Nishizawa, et al., IEEE ED-22 (1975) p.185
4) P.M.Campbell, et al., IEDM Tech. Dig., (1982) p.258
5) P.M.Campbell, et al., IEEEE EDL-6 (1985) p.304
6) A.Cogan, et al., IEDM Tech. Dig., (1983) p.221
7) M.Mori, et al., Japan IEE, 1987 Annual Meeting, Sendai, p.469
8) B.J.Baliga, IEEE ED-29 (1982) p.1560

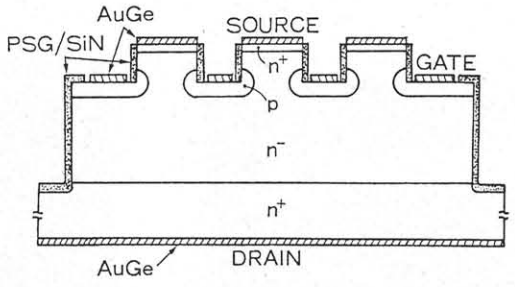
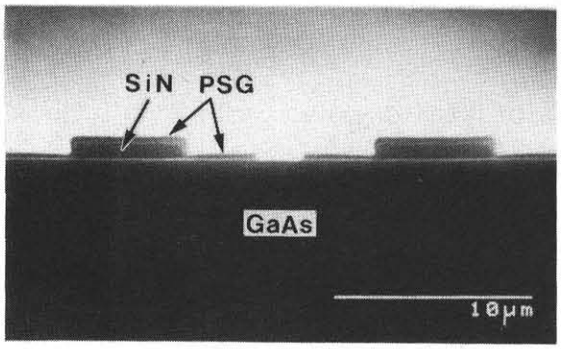
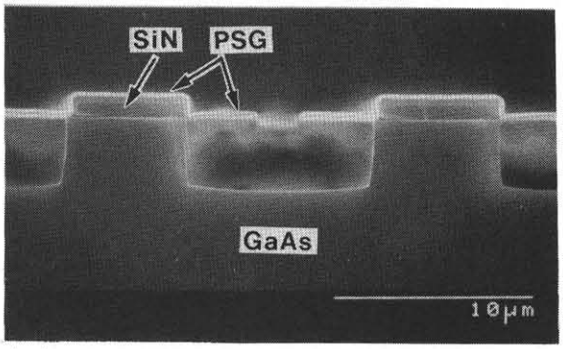


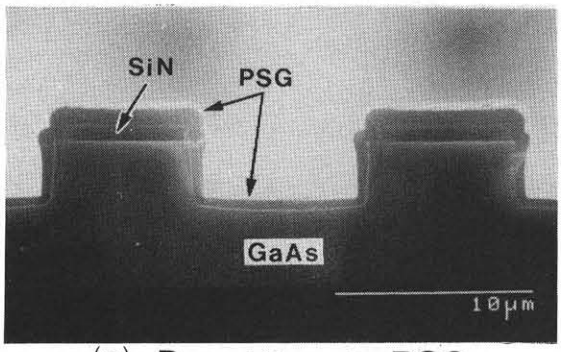
Fig. 1. Recessed gate SIT structure.



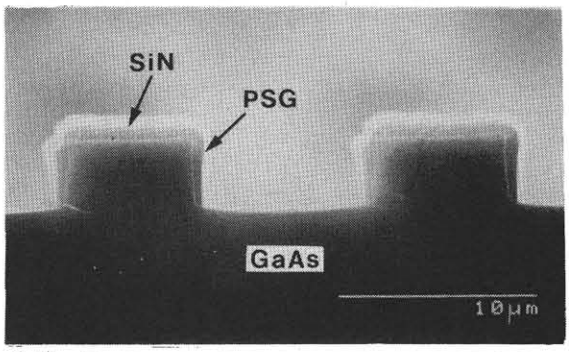
(a) PSG/SiN-etch mask



(b) Anisotropic etching of GaAs

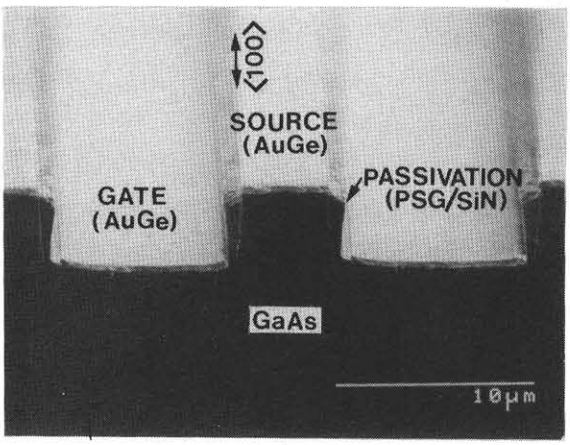


(c) Deposition of PSG

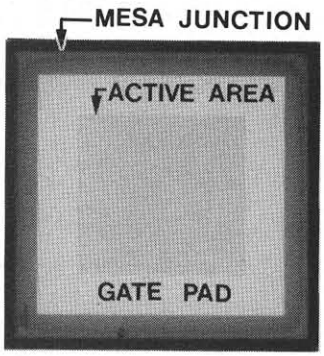


(d) Reactive ion etching of PSG

Fig. 2. Photomicrographs of the recessed gate SIT in the self-aligned fabrication process.

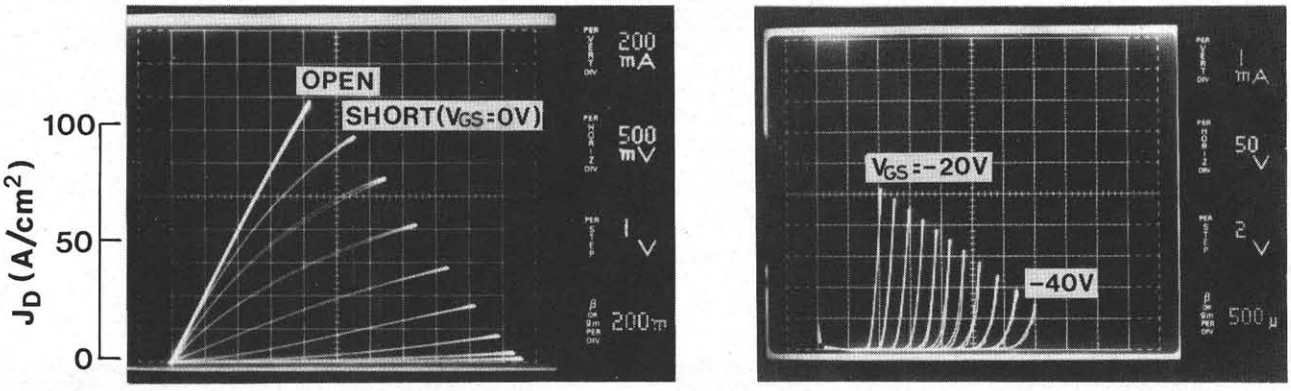


(a) Cross-section



(b) Surface

Fig. 3. Photomicrographs of the recessed gate GaAs SIT. The active area is 1.2mm × 1.2mm.



(a) Output (b) Blocking

Fig. 4. I-V characteristics of GaAs power SIT.

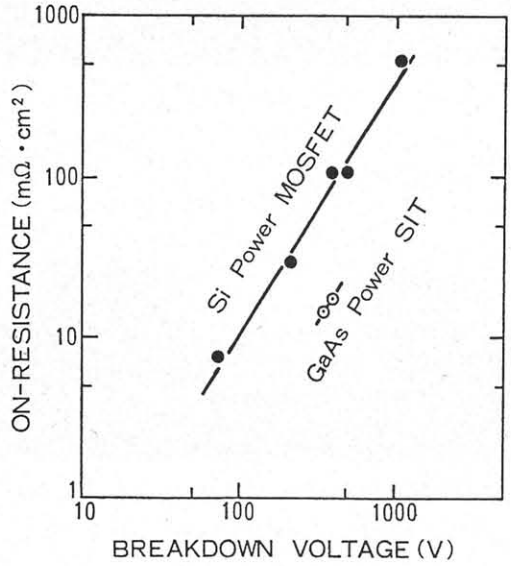


Fig. 5. On-resistance comparison between GaAs power SIT and Si power MOSFET.

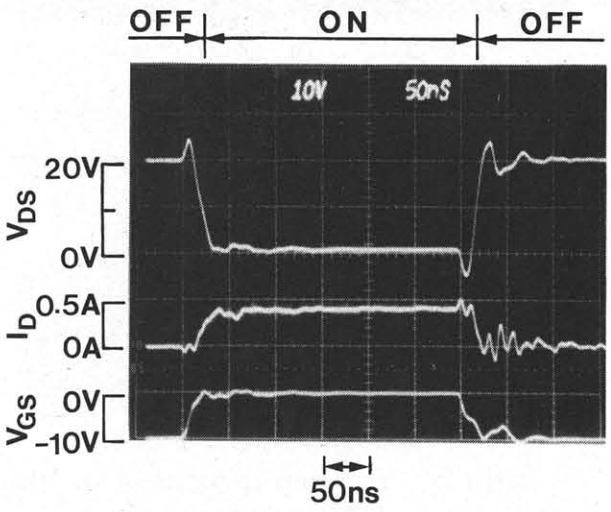


Fig. 6. Switching waveforms for GaAs power SIT.

Table 1. Comparison of electrical characteristics between GaAs power SIT and Si power MOSFET.

Item	GaAs Power SIT	Si Power MOSFET*
Blocking Voltage (V)	400	400
On-resistance (mΩ・cm²)	18	104
Turn-on Time (ns)	20	20
Turn-off Time (ns)	20	45

* Hitachi 2SK 535