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Formation of Arsenic-Implanted PN Junctions Using High Vacuum Ion Implanter

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A new ion implant system has been developed based on the philosophy of Ultra Clean Technology. The system is equipped with an ultra high vacuum implant chamber with a base pressure of 10^{-9} Torr and a ultra clean gas delivery system for ion source, thus eliminating all possible contaminations from the ion implantation process. Arsenic implanted pn junctions annealed at 1000°C exhibited a very low reverse current levels, and their I-V characteristics in the forward and reverse direction were in excellnet agreement with Shockley's equation. The PN junctions subjected to a low temperature anneal at 600°C also exhibited a low leakage current levels of less the 10^{-9}A/cm^2 at a reverse bias voltage of -5V.

1. Introduction

Ion implantation is undoubtedly one of the most essential key technologies in the fabrication of integrated circuits. However, there exist several problems when we try to apply it to Ultra Large Scale Integration (ULSI). High temperatures required to restore the crystallinity of ion implanted layers do not meet the requirement of ULSI processes, i.e., a low temperature processing. It is also quite difficult to form heavily doped regions, without introducing any crystalline defects. In order to solve these problems, we have developed an ultra high vacuum ion implanter in which all possible contamination sources have been almost completely eliminated from the ion implantation process.

The purpose of this paper is to present the basic philosophy to built the system and its application to fabricating P-N junction diodes having ideal forward and reverse current-voltage characteristics which exactly follow the simple Shockley's formula(1).

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2. Ultra High Vacuum Ion Implantation System

Recrystallization of amorphous layers produced by ion implantation proceeds by solid phase epitaxy from the crystalline substrates(2). If there exist any contaminant species in the amorphous layer, they can act as nucleation sites for micro-crystallite formation, thus introducing defects in the recrystallized layer. Solid phase epitaxy strongly depends on temperature, and its rate reduces at low temperatures. As a result, the chance of nucleation and growth of micro-crystallites to occur before the completion of recrystallization becomes much bigger at reduced temperatures. This is why high temperature annealing typically at 900 ∿ 1000°C is required. In order to reduce the annealing temperature without degrading the crystallinity of the implanted layer, it is essentially important to create completely contamination-free environment for ion implantation process. This is the reason why we have developed a new ion implanter having ultra high vacuum capability. In order to realize defect-free heavily doped regions, the concept of stress compensation(3) is also important. Therefore our system is designed so that six different ion speices (As,P,B,Si,Ar,H) can be sequentially implanted without breaking the vacuum.

Figure 1 shows the schematic of the ultra-high vacuum compatible chamber of our system. 1st and 2nd chambers are evacuated by turbo molecular pump and the implant chamber by cryopump which has the base pressure of 10^{-9}Torr. In order to transport wafers in high vacuum without generating dust particles, we have employed a newly developed electrostatic chucking wafer stage system. The holding chuck in the implant chamber firmly holds wafers in a high vacuum by elecrostatic forces thus establishing a good thermal contact between the wafer and the stage as well as the electrical contact to ground the wafer potential. The wafer stage can be cooled down to liquid nitrogen temperature to suppress the annealing during implantation. In order to minimize the contamination from the ion source, ultra clean gas delivery system(4) has been employed for supplying implantation source gases.

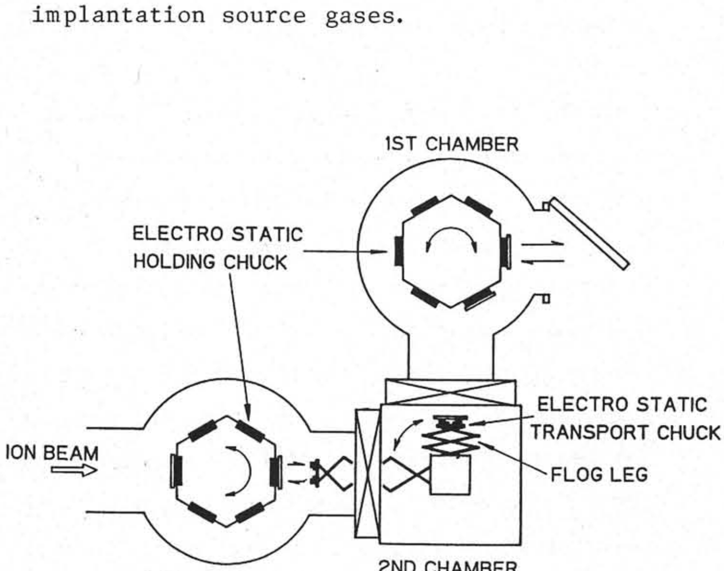

Fig.1 Schematic of the chamber and the wafer transport systems the UHV implanter and the wafer transport.

3. Experimental

0.4 ∿ 0.5 Ω•cm, P-type silicon wafers with (100) orientation were used as starting substrates. The backside of the wafer was p^+ doped prior to the device fabrication. Window patterns of varying sizes were opened in a field oxide which were thermally grown at 1100°C. Arsenic ions were implanted through these windows to form PN junctions in the substrate. Implant doses and energy were 1×10^{15} or $5\times10^{15}cm^{-2}$ and 150KeV, respectively. Implantation was performed either through oxide of 25nm thickness or into bare surfaces. Implanted layers were thermally annealed at 600°C or 1000°C in either N_2 or O_2 ambient. Contact holes were then opened in the CVD oxide of 0.5μm thick. Al electrodes were formed with a phosphorus doped polysilicon(0.2μm) as an intervening barier layer. The whole area of the wafer backside were also metallized by Al to form a good ohmic contact to external electodes. Sintering was carried out at 400°C for 30 minutes in a forming gas ambient.

4. Results and discusions

The solid line in Fig.2 shows the forward current-votage characteristics for a p-n junction diode that was implanted with $5\times10^{15}cm^{-2}$ through the oxide and was annealed at 1000°C for 30 minutes in N_2. The broken line shows the plot of the theoretical values calculated using the Shockley's formura:

$$J=J_0(e^{qV/kT}-1). \quad (1)$$

where J_0 is the saturation current density. It is interesting to note that there is no excess current flowing when the forward bias is reduced to zero. The thoretical curve was best fitted to the experimental data using J_0 as an only fitting parameter. Agreement between the theory and experiment is excellent. The reverse current-voltage characteristics of the same diode is given in Fig.3, where the theoretical curve was calculated by Eq.(1) using J_0 obtained by best fitting of the forward characteristics. Again the agreement is excellent. Such an excellent agreement of the experiment to the Shockley's theory is the result of eliminating contaminations which reduced the number of recombination and generation centers. In order to further examine the agreement between the theory and the experiment, the temperature variation of the reverse current density J_0 was measured. Figure 4 shows the Arhenius plot of J_0 which gives the activation energy of 1.03eV which is nealy equal to the band gap of Si 1.12eV. This suggests that J_0 is given by the diffusion current expressed as

$$J_0=\frac{qn_i^2}{N_A}\sqrt{\frac{D_n}{\tau_n}}. \qquad (2)$$

where D_n and τ_n are the diffusion contact and recombinatopn lifetime of electrons, respectively.The reverse current of this sample exhibits small increase for an increase in the reverse bias voltage due to the generation current which is 5.4×10^{-12} A/cm^2 at 0.1V to 1.5×10^{-11} A/cm^2 at 4.8V due to the generation current. The generation life time(τ_n) of the substrate is roughly estimated as 0.63msec by the using following formula:

$$J_{gen}=qn_i(W-W_0)/\tau_{gen}. \qquad (3)$$

where W is the depletion layer width.

Figure 5 demonstrates the reverse current-voltage characteristics for various annealing conditoins for reverse biases voltages up to -5V. Little increase in generation current component is observed in the sample which was implanted through oxide and annealed at 1000°C. Low reverse current level of 10^{-9} A/cm^2 has been realized in the samples which was annealed at 600°C.

In order to distinguish the peripheral component and the bulk component in the total reverse current density, the reverse current of p-n junctions having various peripheral lengths with the same junction area(1.6×10^{-5} cm^2) were measured. The results were plotted in Fig.6. The recombination life time was calculated from the bulk component using the formula(2) as 8.9μsec and 0.14μsec for 1000°C and 600°C annealed samples, respectively.

5. Conclusions

P-N junctions with extremely low leakage current levels were produced experimentally using ultra high vacuum ion implanter with an electro-static chuking wafer stage. The

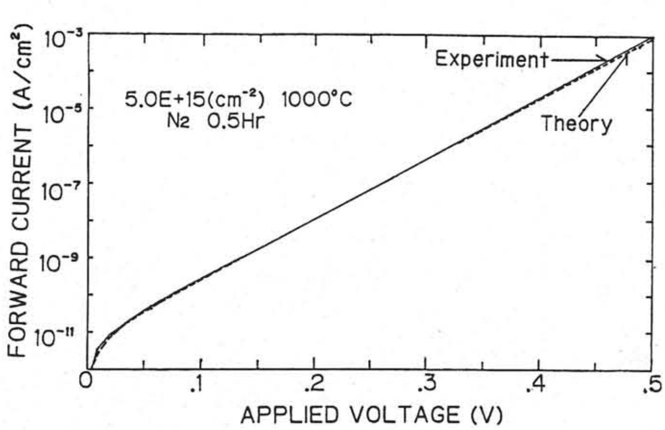

Fig.2 Forward I-V characteristics for pn junction that was implanted with 5×10^{15} cm^{-2} through the oxide and was annealed at 1000°C for 30min in N_2. The junction area is 1.6×10^5 μm^2.

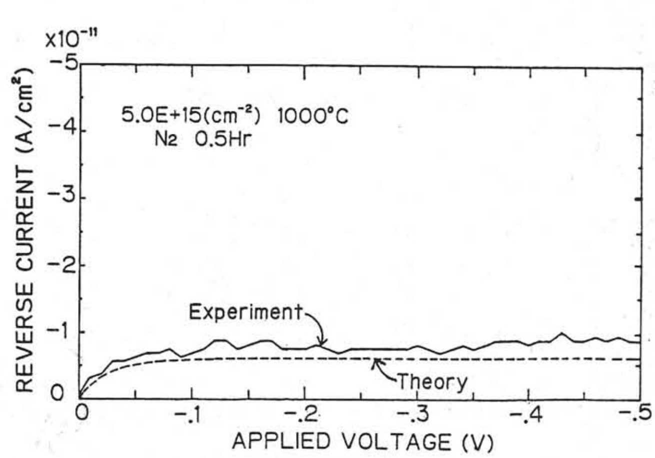

Fig.3 Reverse I-V characteristics for the same sample as in Fig.2.

I-V characteristics of these p-n juncions demonstrated an excellent agreement with Shockley's equation which consists of only diffusion current, since no excess currents were observed flowing in these junctions. Low leakage current levels about 10^{-9} A/cm^2 were also obtained for p-n junctions which were annealed at 600°C. Studies are now being conducted to further reduce the leakage level of low-tempereture annealed P-N junctions by reexamining all possible contamenation sources during processing.

6. Acknowledgement

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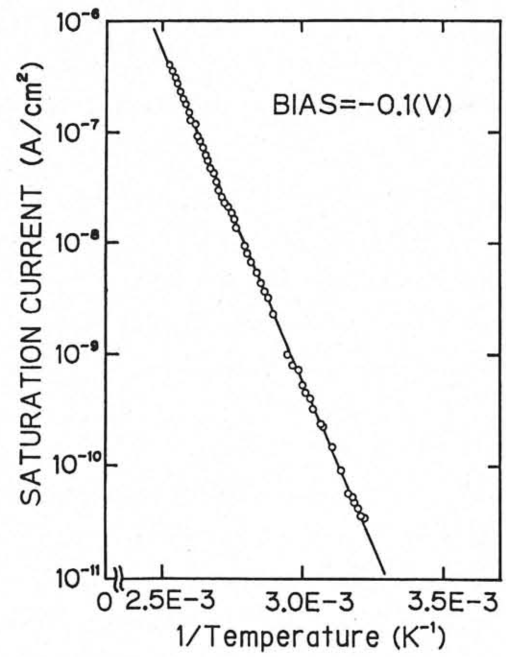

Fig.4 Arhenius plot of J_0.

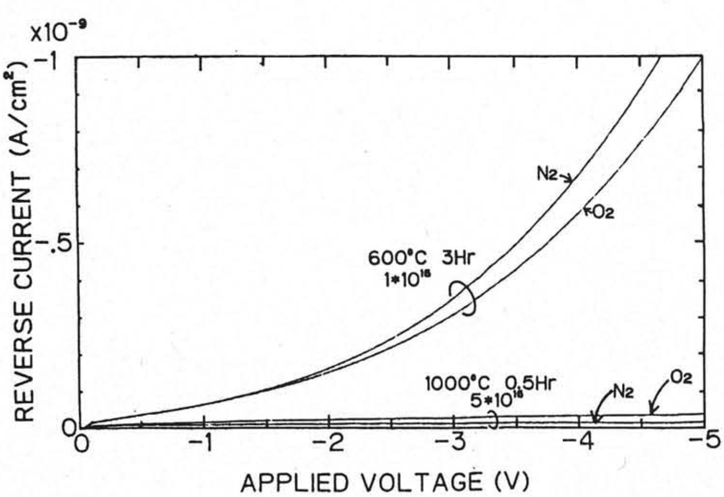

Fig.5 Reverse I-V characteristics for various annealing conditions. The junction area is $4.5\times10^5\ \mu m^2$. The implant doses are 1×10^{15} or 5×10^{15} cm^{-2}.

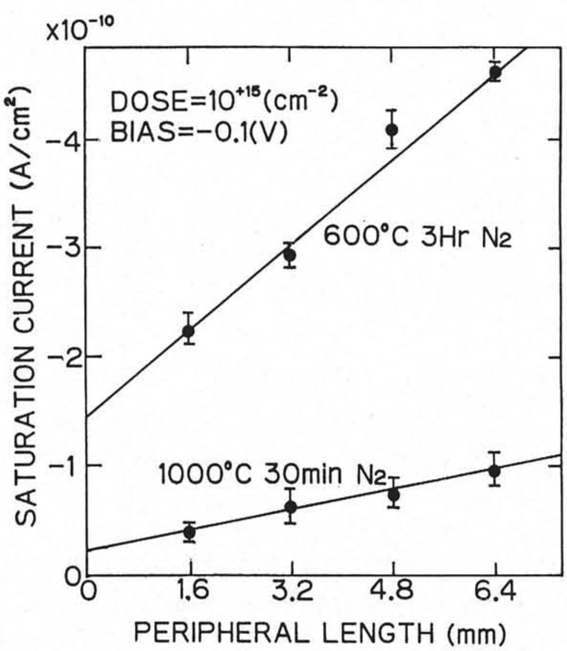

Fig.6 Saturation current versus preipheral length for pn junctions annealed at 1000°C or 600°C