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Doping of Trench Capacitor Cell with As SOG for 4 Megabit DRAM's

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Arsenic doping of trench capacitor cell with arsenic doped spin-on-glass(As SOG)is presented to realize precisely controlled shallow n^+ diffusion layer at vertical trench side walls without inducing great damage. The results from SEM cross sections, doping profiles, damage measurements,C-V characteristics and the punch through voltage measurements between adjacent trench capacitors prove that the As SOG process is promising for realizing 4 megabit DRAM's.

1.Introduction

Trench capacitor cell has been intensively studied for realizing 4 megabit DRAM. One of key processes to trench capacitor cell is impurity doping at the surface of the vertical trench side walls to keep memory storage capacitance and soft error immunity.[1] The major subject in impurity doping of trench capacitor cell is to form precisely controlled shallow n^+ diffusion layer at vertical trench side walls without inducing great damage.

Difficulties with the conventional ion implantation are a large difference[2] in doping concentration and junction depth between trench side walls and the trench bottom, and a great damage induced by ion implantation at high energy. On the other hand, solid phase diffusion is suitable for precisely controlled shallow n^+diffusion layer at vertical trench side walls free from great damage.[3]

In this paper, to form precisely controlled shallow n^+diffusion layer at vertical trench side walls without inducing damage, solid phase diffusion from arsenic doped spin-on-glass (As SOG)is discussed from a view point of process evaluation, such as SEM cross sections, doping profiles,damage measurements, C-V characteristics and the punch through voltage measurements between adjacent trench capacitors,for 4 megabit DRAMs.

2.Experimental

Figure 1 shows the process flow for the trench capacitor cell. After isolation process, deep trenches of typical sizes of 0.9μm diameter and 4um depth were formed with reactive ion etching using CVD SiO2 films as the etching mask. After cleaning of trench surface, a 1.1wt% As SOG was spun on at 3500rpm and then solvents were evaporated at 200°C. Subsequently the shallow n^+ diffusion layer was formed by solid phase diffusion from As SOG at 1000°C for 30 minutes in N2/O2 ambient. The typical surface arsenic concentration in silicon is about $2x10^{19}$ atoms/cm3. The junction depth was 0.15μm. After removing As SOG from the trench surface, thermal SiO2 film was grown for sacrifice oxidation and then removed by wet etching. The capacitor oxide was thermally grown at 1000°C and polysilicon films were filled into the trenches as the cell plate.

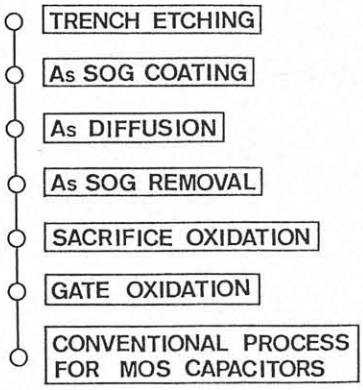

Fig.1 Process flow for trench capacitor cells.

3.Results and discussion

3.1 Doping techniques

Figure 2 shows cross sectional SEM photograps of trenches (a)coated with As SOG and (b)with a shallow n^+ diffusion layer selectively etched. In Fig.2(a), the thickness uniformity of the As SOG on the trench side walls is rather good compared with that on the trench bottom. Typical As SOG thickness on the trench side walls is 60-70nm. Junction depth of n^+diffusion layer were about 0.15μm both at the trench side walls and the trench bottom as shown in Fig.2(b).

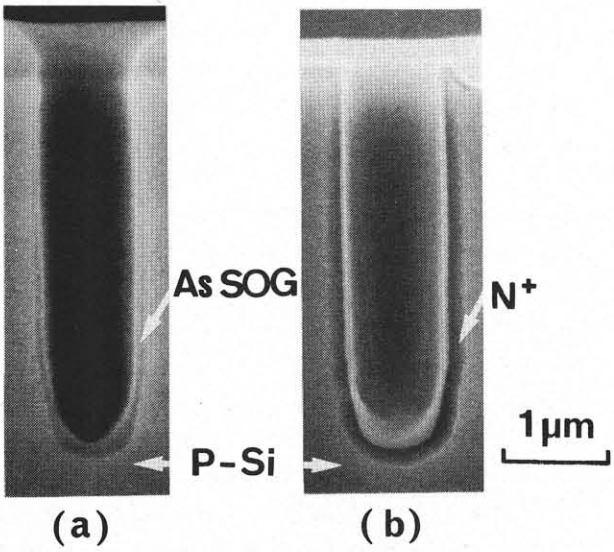

Fig.2 Cross sectional SEM photographs of trenches (a)coated with As SOG and (b)with a shallow n^+diffusion layer selectively etched.

As SOG thickness on the trench side walls is considerably influenced by the trench diameter as indicated in Fig.3. For single coating of As SOG, As SOG thickness on the trench side walls fairly decreases with decreasing in trench diameter, while for double coating of As SOG, As SOG thickness on the trench side walls are more stable in spite of changes in the trench diameter.

Figure 4 shows As SOG thickness dependence of arsenic concentrations and junction depths. Arsenic concentrations tend to increase with increasing the As SOG thickness in each ambient. From Fig.3 and Fig.4, As SOG thickness uniformity on the trench side walls is one of important factors for precisely controlled shallow n^+diffusion.

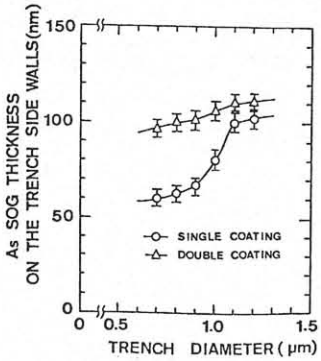

Fig.3 Trench diameter dependence of the As SOG thickness on the trench side walls.

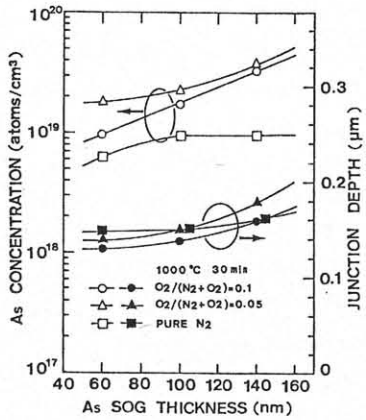

Fig.4 As SOG thickness dependence of arsenic concentration and junction depth.

Figure 5 shows SIMS profiles of arsenic after diffusion from 60nm As SOG. Two arsenic profiles (a) and (b) correspond to the diffusion ambient of O2/(N2+O2)=0.1 and 0.05, respectively. Arsenic surface concentrations of (a) and (b) are about $1x10^{19}$ and $2x10^{19}$ atoms/cm3, respectively.

Figure 6 indicates O2/(N2+O2) ratio dependence of arsenic concentrations and junction depths. Both arsenic concentration and junction depth are very sensitive to O2 flow ratio in the ambient. In particular, arsenic concentration appears to be a maximum in an ambient of O2/(N2+O2)=0.05, enough to prevent the memory cell capacitance decrease.

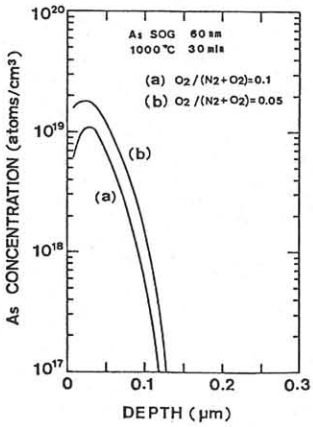

Fig.5 SIMS profiles of arsenic for As SOG.

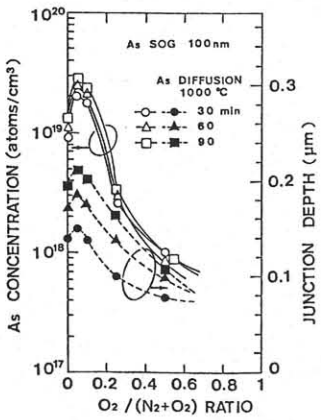

Fig.6 O2/(N2+O2) ratio dependence of arsenic concentration and junction depth.

To evaluate the residual defects after arsenic diffusion from As SOG, a thermal wave technique[4] was used. Figure 7 shows the thermal wave modulated reflectance (TW) signals, which are experimentally correlated with the damage, as a function of O2 flow ratio in diffusion ambient. The TW signal gradually decreases as O2 flow ratio increases. The TW signal for As SOG is relatively low compared with that for arsenic ion implantation at an energy of 40keV and a dose of $5x10^{14}$ /cm2 even after annealing at 1000°C for 20 minutes. These results indicate that arsenic diffusion with As SOG hardly induces residual defects in silicon substrate and is extremely suitable approach to shallow n^+ diffusion layer at vertical trench side walls without inducing great damage.

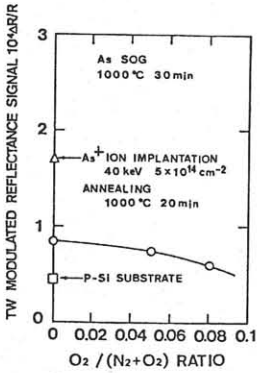

Fig.7 Thermal wave modulated reflectance signal as a function of O2/(N2+O2) ratio.

3.2 Electrical characteristics

Figure 8 shows the efficiency of capacitance utility at -2.5V on cell plate (Cmin/Cox), which is defined as a ratio of the storage capacitance at -2.5V on cell plate to the satulation capacitance in an accumulation mode, as a function of O2 flow ratio in arsenic diffusion ambient. For single coating of As SOG, the capacitance efficiency (Cmin/Cox) increases up to 0.75 with decreasing the O2 flow ratio. Double coating of As SOG in more effective with 0.85. For arsenic ion implantation, the capacitance efficiency falls below 0.5.

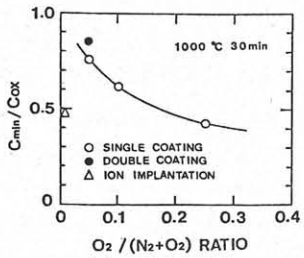

Fig.8 Efficiency of capacitance utility at -2.5V on cell plate(Cmin/Cox) as a function of O2/(N2+O2) ratio in arsenic diffusion ambient.

In order to characterize the electrical isolation between adjacent trenches, different spacings were fabricated by varying the trench to LOCOS distance. Figure 9 shows a schematic cross section of a test structure for punch through voltage measurements between adjacent trenches formed in a p-well with 0.9μm diameter and 4um depth.

Figure 10 shows results of punch through voltage measurements between adjacent trenches. The cell plate voltage at 10^{-12} A trench to trench leakage current remarkably depends on the cell to cell separation. The cell plate voltage for the samples with As SOG is higher by 3V at 1.8μm cell to cell separation due to the precisely controlled shallow n^+ diffusion without damage both at vertical trench side walls and the trench bottom.

To examine a feasibility of arsenic doping with As SOG, the As SOG process is applied to 4 megabit DRAM. The pause refresh time of 4 megabit DRAM with As SOG proves to be 50-100 seconds which implies leakage current between adjacent trenches is sufficiently small.

4.Conclusion

Arsenic doping of trench capacitors with As SOG have been discussed in terms of doping techniques and electrical characteristics .

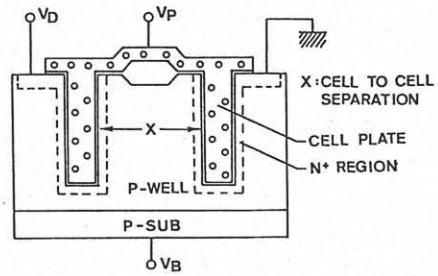

Fig.9 Schematic cross section of punch through test structure between adjacent trenches.

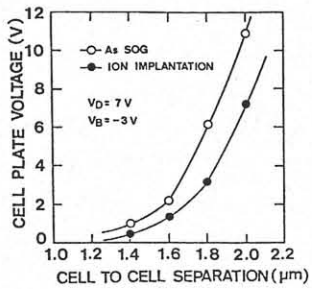

Fig.10 Punch through voltage measurements between adjacent trenches.

Precisely controlled shallow n^+ diffusion layer at vertical trench side walls is realized without great damage and presents punch through between adjacent trenches resulting in superior pause refresh time characteristics.

Consequently, As SOG process is promising for realizing 4 megabit DRAMs with the deep trench capacitors.

Acknowledgments

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References

1. H.Binder,H.Geiger,R.Kakoschke,H.M. Mühlhoff and S.Röhl:Extended Abstructs of the 18th Conference on Solid State Device and Materials (1986) p.299.
2. G.Fuse,H.Umimoto,S.Odanaka, M.Wakabayashi,M.Fukumoto and T.Ohzone :J.Electrochem.Soc. 133 (1986) 996.
3. K.Yamada,K.Yamabe,Y.Tsunashima, K.Imai,T.Kashio and H.Tango:IEDM Tech. Dig. (1985) p.702.
4. J.Opsal,M.W.Taylor,W.L.Smith and A.Rosencwig:J.Appl.Phys. 61 (1987) 240.