Arsemic Diffusion from Solid Source and Its Application to Trench Capacitor

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The technique of arsenic diffusion from a solid source into inner surface of Si trench was examined and the feasibility of applying to the technique of trench capacitor was demonstrated. We have achieved diffusion depth as low as 0.15um and surface density as high as $2 \times 10^{12}/\text{cm}^2$. Thin SiO$_2$ on As layer has defect density as low as that of non-doped substrate. Though the trench to trench spacing is 1.4um, the leakage current through the trench wall is small enough indicating the feasibility of using this technique for 4Mbits DRAM.

1. Introduction

In order to realize high density MOS-DRAM greater than 1Mbits, we have to reduce the memory cell area, especially the storage capacitor area. One effective approach is adopting trench capacitor, which is able to be increasing the effective capacitor area. To fabricate electrode plate in the trench, high doped layer in the trench surface is needed. The trench capacitor has been developed with various structures. Ion implantation, spin-on glass method and AsSG-CVD technique have been tested to form shallow and highly doped As layer. However, these methods have difficult problems in themselves. We have developed the technique of As diffusion from a solid source into the wall of Si trench.

This paper describes the basic properties of As diffused layer by this technique, and the electrical properties of thin dielectric film, namely SiO$_2$ or SiO$_2$/SiN/SiO$_2$ stacked film on the As diffused layer. Further it describes on the operation of the memory cell fabricated by this technique.

2. Experimental

As diffusion from the solid source proceeds in the following chemical reaction.

$$2\text{AlAsO}_4 \rightarrow \text{Al}_2\text{O}_3 + \text{As}_2\text{O}_3 + \text{O}_2$$

As$_2$O$_3$ and O$_2$ are vaporized and reach the surface of substrate. AssG grows on Si surface and As diffuses into Si. The solid sources in disk form and the Si wafers were set face to face in the quartz tube in 900-1000 °C for 30-60 minutes. The Si wafer is 10-15 ohm-cm in resistivity in case for P-type (100) and 3-6 ohm-cm for N-type (100). The trench was formed in the depth of 2um to 4um and with the width of 1.2 um to 2.3um by RIE.

The depth of As diffused layer of the Si surface was measured for plots by secondary ion mass spectroscopy (SIMS) and the technique of stain after angle lapping. The depth of As layer of the trench surface was measured by scanning electron microscope (SEM) observation on the cross section of trench.

As diffused MOS capacitor was fabricated on P(100) or N(100) CZ Si substrate with and without trench simultaneously. SiO$_2$ or
**SiO₂/SiN/SiO₂** were examined on dielectric film of MOS capacitor. The SiO₂ layer, 9.0-15.0 nm thick, was thermally grown in dry O₂/HCl or dry O₂ ambient at 900-950 °C. SiO₂/SiN/SiO₂ stacked film was fabricated with thermally grown SiO₂ and SiN deposited by LPCVD. The capacitance of the stacked dielectric film is equal to that of 9.5 nm SiO₂ capacitor. Poly Si electrode area was 0.16-4 mm². SiO₂ thickness was measured by an ellipsometry and from C-V curves. From dielectric breakdown characteristics of SiO₂ and SiO₂/SiN/SiO₂, defect density of these films were estimated assuming that it follows the poisson's distribution and that yield of MOS capacitor fabrication was defined by the number of capacitors having breakdown field over 8 MV/cm.

The leakage current of the junction of As layer was measured both on trench and no trench types. The leakage current between neighboring trenches was measured on the trenches 750 um in length and separated by over 0.8 um.

### 3. Results

#### 3-1. As diffused layer

Table 1 shows the depth and the surface concentration of As diffused layer under various diffusion temperatures. Under the condition of 1000 °C and 30 minutes, the depth of As layer is 0.15 um and the surface concentration has been measured as 8EXP19/cm³ by SIMS and 2EXP20/cm³ by C-V method. Uniformity of sheet resistance on 4" wafer is within ±5 % in the concentration range of 2EXP19/cm³ to 2EXP20/cm³.

![Fig. 1 Cmin/Cmax of MOS with and without trench](image1.png)

**Fig. 1** Cmin/Cmax of MOS with and without trench

![Fig. 2 Dependence of Cmin/Cmax on trench depth](image2.png)

**Fig. 2** Dependence of Cmin/Cmax on trench depth

![As diffused layer](image3.png)

**Photo 1 Cross sectional view of SiN on As diffused layer in trench**

formed on the plane Si. Moreover, in Fig. 2 there is no dependence of Cmin/Cmax on trench depth from 2 um to 4 um, and the value of these Cmin/Cmax is same level as that of plane Si. Therefore it is clear that As diffusion from solid source is able to

### Table 1

<table>
<thead>
<tr>
<th>As Diffusion</th>
<th>Depth</th>
<th>Surface concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp (°C)</td>
<td>Time (min)</td>
<td>Xj(µm)</td>
</tr>
<tr>
<td>950</td>
<td>30</td>
<td>0.08</td>
</tr>
<tr>
<td>975</td>
<td>30</td>
<td>0.18</td>
</tr>
<tr>
<td>1000</td>
<td>30</td>
<td>0.15</td>
</tr>
</tbody>
</table>
form high doped As layer with good uniformity even in deep trench as well as plane Si.

Photo 1 shows cross sectional view of As diffused layer by SEM observation. It seems that the depth of diffused layer has good uniformity along the inner surface of the trench.

As for the electrical property of As layer, the leakage current of the As layer/substrate junction is less than $3 \times 10^{-9}$ A/cm$^2$ at 6V, which is the same level as that of the junction made by conventional doping method such as ion implantation.

From chemical reaction (1), the existence of Al in As diffused layer was expected. However, from the results of SIMS analysis, the concentration of Al in Si substrate was less than the limitation of measurement.

3-2 Thin dielectric film on As diffused layer

The dependence of thermally grown SiO$_2$ thickness upon the surface concentration of As is shown in Fig. 3. As the surface concentration of As increases, SiO$_2$ thickness increases. With the oxidation condition of 9.0 nm SiO$_2$ thickness on nondoped substrate P(100), SiO$_2$ grows to 9.5 nm when the As surface concentration is $2 \times 10^{20}$/cm$^3$. The uniformity of SiO$_2$ thickness on 4" As diffused Si wafer is within ±5%.

I-V characteristics of SiO$_2$ on As layer are shown in Fig. 4. Negative bias applied on poly Si electrode. Regardless of presence of As layer, Fowler-Nordheim tunneling current through SiO$_2$ is observed and barrier height $\Phi_B$ (3.2-3.3 eV) with positive bias is the same value as that with negative bias.

In Fig. 5, oxide breakdown characteristics are shown. From these results, the oxide defect density with As diffusion is the same as that with no As diffusion. On the other hand, the stacked dielectric film of SiO$_2$/SiN/SiO$_2$ structure, which is expected to have high reliability as thin dielectric film for memory capacitor, was evaluated for dielectric breakdown characteristic and defect density. The results are shown in Fig. 6. Comparing SiO$_2$/SiN/SiO$_2$ with SiO$_2$ in 3 um depth trench, SiO$_2$/SiN/SiO$_2$ has less defect density than SiO$_2$. Moreover, the defect density of SiO$_2$/SiN/SiO$_2$ is lower than 1/cm$^2$, and is independent of trench depth in the range of 2 um to 4 um.

Time dependent dielectric breakdown (TDDB) of SiO$_2$ and SiO$_2$/SiN/SiO$_2$ was measured (Fig. 7). Time to 50% failure of SiO$_2$ and SiO$_2$/SiN/SiO$_2$ on As layer is shorter than that on non As layer. But SiO$_2$/SiN/SiO$_2$ film has longer life than SiO$_2$. Reliability of SiO$_2$/SiN/SiO$_2$ on As layer seems to be the
same as that of SiO₂ on non As diffused layer.

3-3 Memory cell operation

Fig. 8 shows the plot of voltage Vdth at 1 nA trench to trench punch through current. Each trench has 750 um length. S shows trench to trench separation. The concentration of P well is 2EXP16/cm³ at trench bottom. From Fig. 8, it is evident that for As doped trenches punch through occurs at operating voltage (in this case >6 V) with a minimum separation of 1.4 um when substrate concentration is greater than 2EXP16/cm³.

Basic memory cell operation was examined for the experimentally fabricated trench capacitor cell in the simple test circuit shown in Fig. 9, where wave-forms for basic memory cell operation are shown.

4. Summary

The basic properties of As diffusion from solid source were studied on plane Si and trench Si. High surface concentration and shallow depth of As layer were able to form in the trench. The electrical properties of junction layer and thin dielectric film on the As layer were satisfactory for use in memory applications. Memory cell operation was demonstrated. From above results, it is verified that the technique of As diffusion from solid source is well applicable to fabricate megabit MOS-DRAMs.

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6. Reference

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