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C-8-3

Arsenic Diffusion from Solid Source and Its Application to Trench Capacitor

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The technique of arsenic diffusion from a solid source into inner surface of Si trench was examined and the feasibility of applying to the technique of trench capacitor was demonstrated. We have achieved diffusion depth as low as 0.15um and surface density as high as 2EXP20/cm3. Thin SiO_2 on As layer has defect density as low as that of non doped substrate. Though the trench to trench spacing is 1.4um, the leakage current through the trench wall is small enough indicating the feasibility of using this technique for 4Mbits DRAM.

1. Introduction

In order to realize high density MOS-DRAM greater than 1Mbits, we have to reduce the memory cell area, especially the storage capacitor area. One effective approach is adopting trench capacitor, which is able to be increasing the effective capacitor area. To fabricate electrode plate in the trench, high doped layer in the trench surface is needed. The trench capacitor has been developed with various structures. Ion implantation, spin-on glass method and AsSG-CVD technique have been tested to form shallow and highly doped As layer. However, these methods have difficult problems in themselves. We have developed the technique of As diffusion from a solid source into the wall of Si trench.

This paper describes the basic properties of As diffused layer by this technique, and the electrical properties of thin dielectric film, namely SiO_2 or $SiO_2/SiN/SiO_2$ stacked film on the As diffused layer. Further it describes on the operation of the memory cell fabricated by this technique.

2. Experimental

As diffusion from the solid source proceeds in the following chemical reaction.

$$2AlAsO_4 \text{ ------> } Al_2O_3+As_2O_3+O_2 \quad (1)$$

As_2O_3 and O_2 are vaporized and reach the surface of substrate. AsSG grows on Si surface and As diffuses into Si. The solid sources in disk form and the Si wafers were set face to face in the quartz tube in 900-1000 °C for 30-60 minutes. The Si wafer is 10-15 ohm-cm in resistivity in case for P-type (100) and 3-6 ohm-cm for N-type (100). The trench was formed in the depth of 2um to 4um and with the width of 1.2 um to 2.3um by RIE.

The depth of As diffused layer of the Si surface was measured for plots by secondary ion mass spectroscopy (SIMS) and the technique of stain after angle lapping. The depth of As layer of the trench surface was measured by scanning electron microscope (SEM) observation on the cross section of trench.

As diffused MOS capacitor was fabricated on P(100) or N(100) CZ Si substrate with and without trench simultaneously. SiO_2 or

$SiO_2/SiN/SiO_2$ were examined on dielectric film of MOS capacitor. The SiO_2 layer, 9.0-15.0 nm thick , was thermally grown in dry O_2/HCl or dry O_2 ambient at 900-950 ℃. $SiO_2/SiN/SiO_2$ stacked film was fabricated with thermally grown SiO_2 and SiN deposited by LPCVD. The capacitance of the stacked dielectric film is equal to that of 9.5 nm SiO_2 capacitor. Poly Si electrode area was 0.16-4 mm^2. SiO_2 thickness was measured by an ellipsometry and from C-V curves. From dielectric breakdown characteristics of SiO_2 and $SiO_2/SiN/SiO_2$, defect density of these films were estimated assuming that it follows the poisson's distribution and that yield of MOS capacitor fabrication was defined by the number of capacitors having breakdown field over 8 MV/cm.

The leakage current of the junction of As layer was measured both on trench and no trench types. The leakage current between neighboring trenches was measured on the trenches 750 um in length and separated by over 0.8 um.

3. Results

3-1. As diffused layer

Table 1 shows the depth and the surface concentration of As diffused layer under various diffusion temperatures. Under the condition of 1000 ℃ and 30 minutes, the depth of As layer is 0.15 um and the surface concentration has been measured as 8EXP19/cm^3 by SIMS and 2EXP20/cm^3 by C-V method. Uniformity of sheet resistance on 4" wafer is within ±5 % in the concentration range of 2EXP19/cm^3 to 2EXP20/cm^3.

Fig. 1 and Fig. 2 show the Cmin/Cmax on the C-V curve of the As diffused layers. Fig. 1 indicates that the value of Cmin/Cmax with trench is equal to that without trench. This fact suggests that the surface concentration of As diffused layer formed in the inner surface of trench is equal to that

As Diffusion		Depth	Surface concentration	
Temp (℃)	Time (min)	Xj (μm)	SIMS (/cm^3)	C-V (/cm^3)
950	30	0.08	2E19	2E19
975	30	0.13	4E19	6E19
1000	30	0.15	8E19	2E20

Table 1
Xj and Surface Concentration of As Diffution Layer

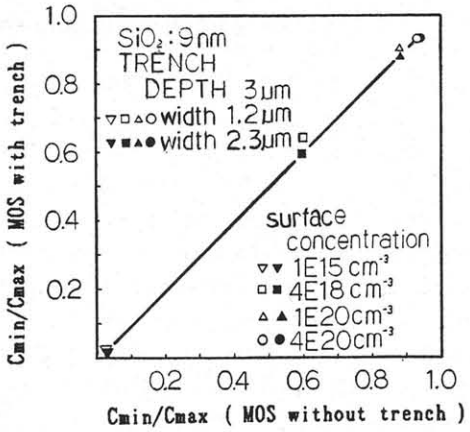

Fig. 1 Cmin/Cmax of MOS with and without trench

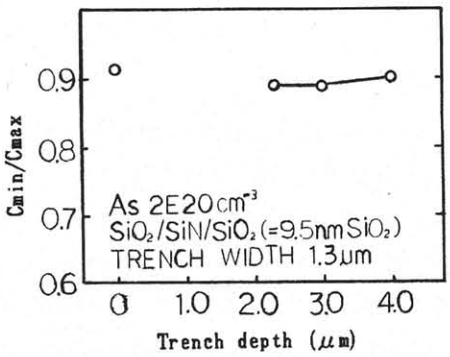

Fig. 2 Dependence of Cmin/Cmax on trench depth

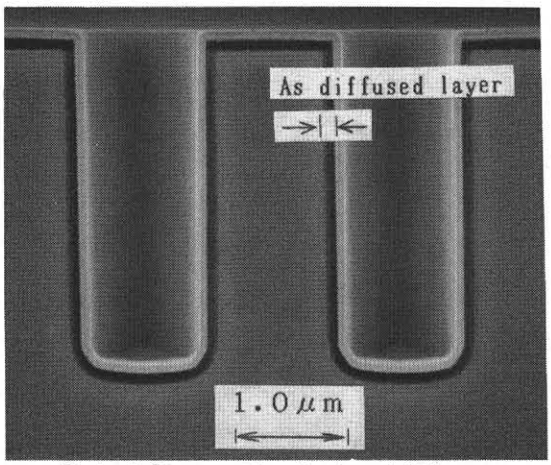

Photo 1 Cross sectional view of SEM on As diffused layer in trench

formed on the plane Si. Moreover, in Fig. 2 there is no dependence of Cmin/Cmax on trench depth from 2 um to 4 um, and the value of these Cmin/Cmax is same level as that of plane Si. Therefore it is clear that As diffusion from solid source is able to

form high doped As layer with good uniformity even in deep trench as well as plane Si.

Photo 1 shows cross sectional view of As diffused layer by SEM observation.
It seems that the depth of diffused layer has good uniformity along the inner surface of the trench.

As for the electrical property of As layer, the leakage current of the As layer/substrate junction is less than 3EXP-9 A/cm^2 at 6V, which is the same level as that of the junction made by conventional doping method such as ion implantation.

From chemical reaction (1), the existence of Al in As diffused layer was expected. However, from the results of SIMS analysis the concentration of Al in Si substrate was less than the limitation of measurement.

3-2 Thin dielectric film on As diffused layer

The dependence of thermally grown SiO_2 thickness upon the surface concentration of As is shown in Fig. 3. As the surface concentration of As increases, SiO_2 thickness increases. With the oxidation condition of 9.0 nm SiO_2 thickness on nondoped substrate P(100), SiO_2 grows to 9.5 nm when the As surface concentration is 2EXP20/cm3. The uniformity of SiO_2 thickness on 4" As diffused Si wafer is within ± 5 %.

I-V characteristics of SiO_2 on As layer are shown in Fig. 4. Negative bias applied on poly Si electrode. Regardless of presence of As layer, Fowler-Nordheim tunneling current through SiO_2 is observed and barrier height ϕB (3.2-3.3 eV) with positive bias is the same value as that with negative bias.

In Fig. 5, oxide breakdown characteristics are shown. From these results, the oxide defect density with As diffusion is the same as that with no As diffusion. On the other hand, the stacked dielectric film of $SiO_2/SiN/SiO_2$ structure, which is expected to have high reliability as thin dielectric film for memory capacitor, was evaluated for dielectric breakdown characteristic and defect density. The results are shown in Fig. 6. Comparing $SiO_2/SiN/SiO_2$ with SiO_2 in 3 um depth trench, $SiO_2/SiN/SiO_2$ has less defect density than SiO_2. Moreover, the defect density of $SiO_2/SiN/SiO_2$ is lower than 1/cm^2, and is independent of trench depth in the range of 2 um to 4 um.

Time dependent dielectric breakdown (TDDB) of SiO_2 and $SiO_2/SiN/SiO_2$ was measured (Fig. 7). Time to 50 % failure of SiO_2 and $SiO_2/SiN/SiO_2$ on As layer is shorter than that on non As layer. But $SiO_2/SiN/SiO_2$ film has longer life than SiO_2. Reliability of $SiO_2/SiN/SiO_2$ on As layer seems to be the

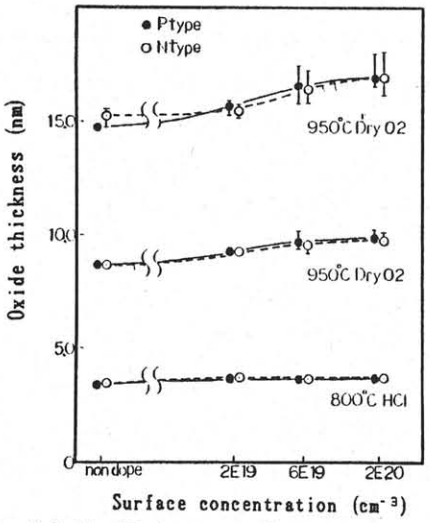

Fig. 3 Oxide thickness vs. Surface concentration

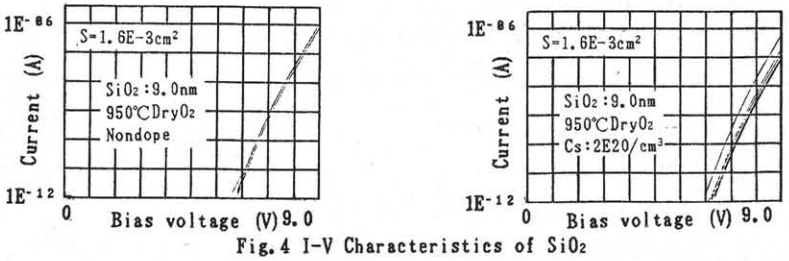

Fig. 4 I-V Characteristics of SiO_2

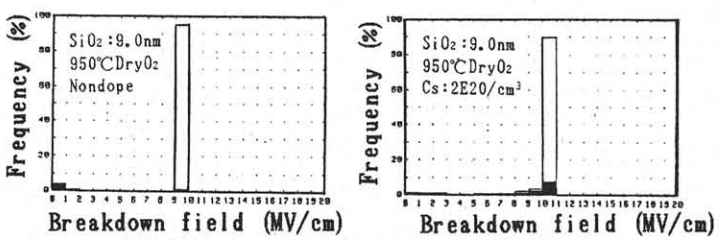

Fig. 5 Oxide breakdown voltage histograms

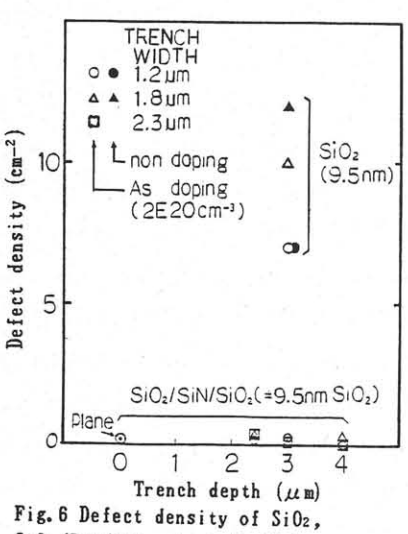

Fig. 6 Defect density of SiO_2, $SiO_2/SiN/SiO_2$ stacked dielectric film

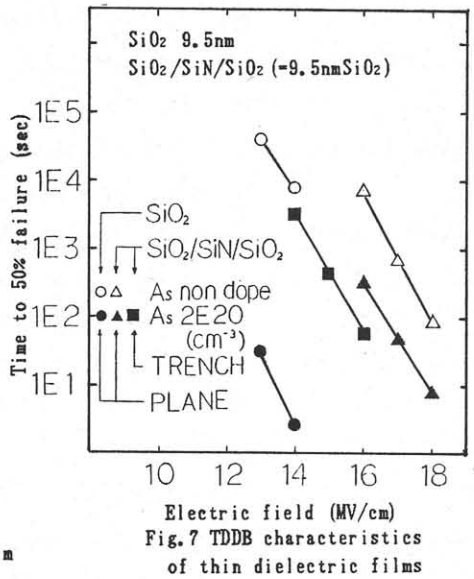

Fig. 7 TDDB characteristics of thin dielectric films

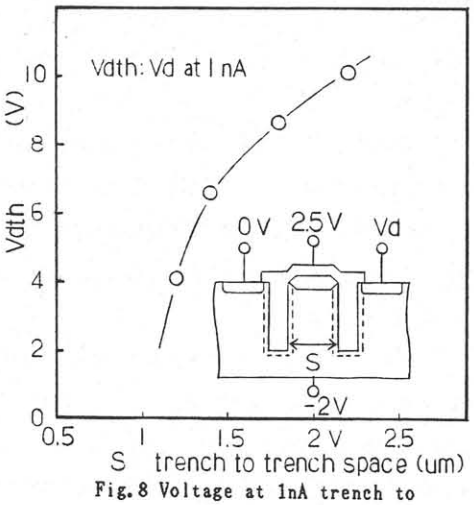

Fig. 8 Voltage at 1nA trench to trench leakage current

same as that of SiO_2 on non As diffused layer.

3-3 Memory cell operation

Fig.8 shows the plot of voltage Vdth at 1 nA trench to trench punch through current. Each trench has 750 um length. S shows trench to trench separation. The concentration of P well is 2EXP16/cm3 at trench bottom. From Fig. 8, it is evident that for As doped trenches punch through occurs at operating voltage (in this case ; >6 V) with a minimum separation of 1.4 um when substrate concentration is greater than 2EXP16/cm3.

Basic memory cell operation was examined for the experimentally fabricated trench capacitor cell in the simple test circuit shown in Fig. 9, where wave-forms for basic memory cell operation are shown.

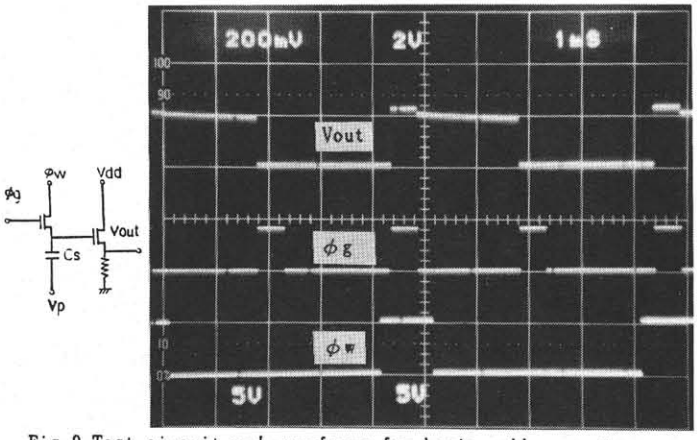

Fig. 9 Test circuit and waveforms for basic cell operation

4. Summary

The basic properties of As diffusion from solid source were studied on plane Si and trench Si. High surface concentration and shallow depth of As layer were able to form in the trench. The electrical properties of junction layer and thin dielectric film on the As layer were satisfactory for use in memory applications. Memory cell operation was demonstrated. From above results, it is verified that the technique of As diffusion from solid source is well applicable to fabricate megabit MOS-DRAMs.

5. Acknowledgments

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6. Reference

(1) N. Matsuo, et al., Extended Abstracts (The 34th Spring Meeting, 1987); The Japan Society of Applied Physics and Related Societies, 30a-c-1.