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A 20 ps/G Si Bipolar IC Using Advanced SST with Collector Ion Implantation

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This paper describes SST-1B (Super Self-aligned process Technology) using Selectively Ion-implanted Collector (SIC) process, which is an advanced version of SST-1A in high speed Si bipolar LSI. The SIC is a new process to improve shallow base-collector profiles to reduce base width and intrinsic base resistance, and to suppress the base pushout effect (Kirk's effect) in the high current mode. The profiles are easily controlled by 150 - 200 KeV phosphorus ion implantation at the base-collector junction. Using this process, SST-1B has achieved a high cut-off frequency of 21.1 GHz - 25.7 GHz and a fast switching delay of 20.5 ps/G for non-threshold logic and 34.1 ps/G for emitter-coupled logic. SST-1B has potential applications to 50 ps/G logic LSI and 10 GHz SSI.

1. INTRODUCTION

Si bipolar devices have been advanced to the point where sub-100 ps/G logic LSIs and sub-ns RAMs are available for mainframe computers, and gigabit logic ICs for optical fiber systems. To achieve high speed operation, several self-aligned bipolar technologies have been developed to scale down the whole lateral feature size and to reduce the parasitic capacitances and resistances.

However, the vertical scale-down of the bipolar devices to achieve a high cut-off frequency (f_T) is not progressing rapidly. Because the intrinsic base layer is usually formed by ion implantation in high speed bipolar technology, it is hardly possible to avoid spreading the base profile owing to the channeling effect. The channeling effect has been a barrier to the vertical scaling-down to reduce both the base width (W_B) and the intrinsic base resistance (R_{bb}).

Therefore, SST-1B, which is an advanced version of SST-1A[1] (Super Self-aligned process Technology), has been developed using a Selectively Ion-implanted Collector (SIC) process to raise the cut-off frequency and to reduce the intrinsic base resistance by improvement on the base-collector profiles, and to increase the switching speed of Si LSIs.

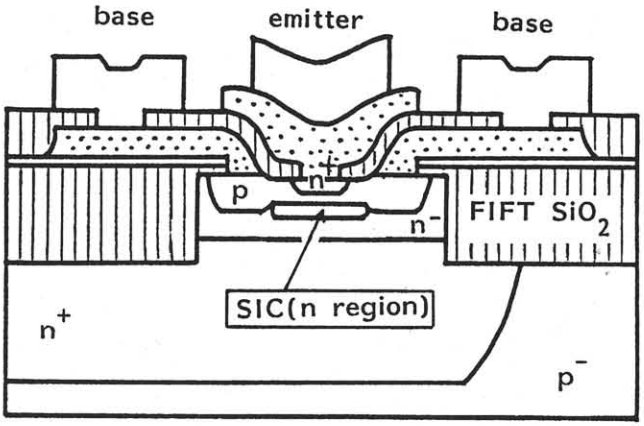

Fig.1 Cross-sectional view of SST-1B transistor with SIC using FIFT (Fine Isolation Frame Trench).

In this presentation, SST-1B structure with SIC, device analysis and experimental results on cut-off frequency and basic propagation delays (t_{pd}) of non-threshold logic (NTL) and emitter-coupled logic (ECL) are described.

2. DEVICE STRUCTURE

A schematic structure of the SST-1B transistor with SIC using a new isolation technology of FIFT (Fine Isolation by Frame Trench) is shown in Fig.1. The SIC process, whereby phosphorus ions are selectively implanted at the base-collector junction, forms the N region between the intrinsic base and the N^- epitaxial layer. The N region can be selectively located just under the emitter area by taking advantage of the cross-sectional shape peculiar to SST-1B structure whereby the external base region is masked for ion implantation with a thick base polysilicon electrode, so there is no increase in collector capacitance in the external base region.

3. DEVICE ANALYSIS

An impurity profile under emitter area with SIC shown in Fig.2 was used for device simulation. The profile shows that the channeling tail in the base layer is compensated by the collector ion implantation. The base width with SIC then becomes 1.5 or 2 times smaller than the conventional width.

Another advantage of SIC is that R_{bb} can be reduced by higher dose base ion implantation, even though the base width is thinner, when the optimum process condition for base and collector ion implantation is chosen. It means that advanced SST-1B achieves higher f_T and lower R_{bb} at the same time.

To estimate the base pushout effect (Kirk's effect[2]) in the high current mode, electron and hole carrier profiles were simulated. The carrier profiles with and without SIC are shown in Figs.3-a and 3-b. The hole profile without SIC clearly indicates base pushout and effective base width ($W_{B(eff)}$) widening, as shown in Fig.3-b. Conversely, Figure 3-a shows that base pushout is suppressed at the N layer formed by SIC.

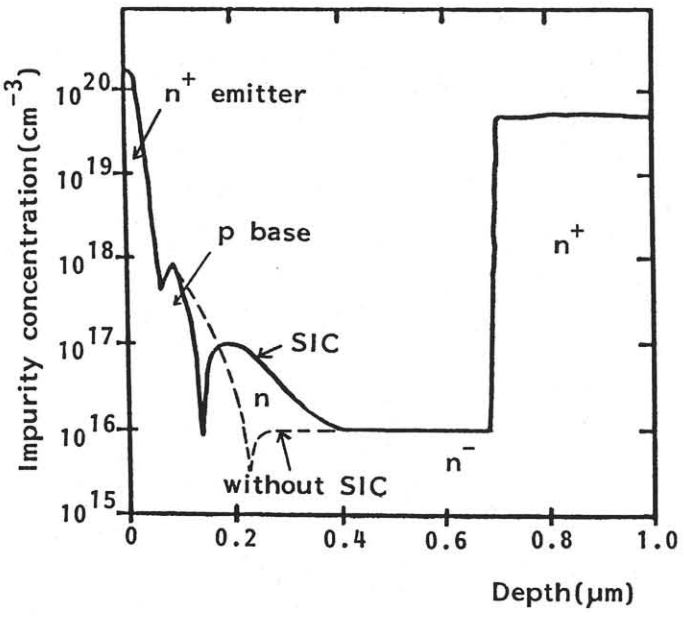

Fig.2 Impurity profile with SIC for device simulation.

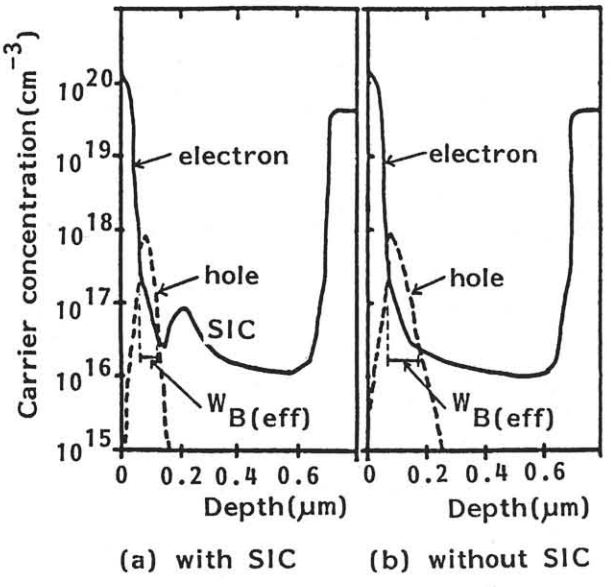

Fig.3 Calculated carrier profiles (a) with SIC and (b) without SIC at high current density of 40 KA/cm^2. The effective base width ($W_{B(eff)}$) changes when SIC is present.

As a result, The maximum cut-off frequency (f_{TMAX}) and the current density increase concurrently.

4. PROCESS

To evaluate the effects of SIC process, SST-1B transistors with SIC and ring oscillators were fabricated. The transistor had a 0.35 μm emitter and 1.6 μm base region. The process flow is shown in Fig.4, and is almost the same as previously reported [3] with the exception of selective collector ion implantation.

(1) After N^+ diffusion and 0.9 μm N^- epitaxial growth, FIFT was used as isolation technology which consists of Si reactive ion etching and CVD-SiO_2 filling-up in the field. The CVD-SiO_2 is 1 μm thick.

(2) The P^+ base polysilicon electrodes, its contacts to Si substrate and thin oxide film on intrinsic area are formed as previously reported.

(3) Both base and collector ion implantations were done in SIC fabrication. Due to a very shallow base in a high speed bipolar transistor, it is easy for a common ion implanter to dope phosphorus into the base-collector junction at 150 - 200 KeV.

(4) After emitter diffusion from arsenic ion-implanted polysilicon and two level metallization, the SST-1B process was finished.

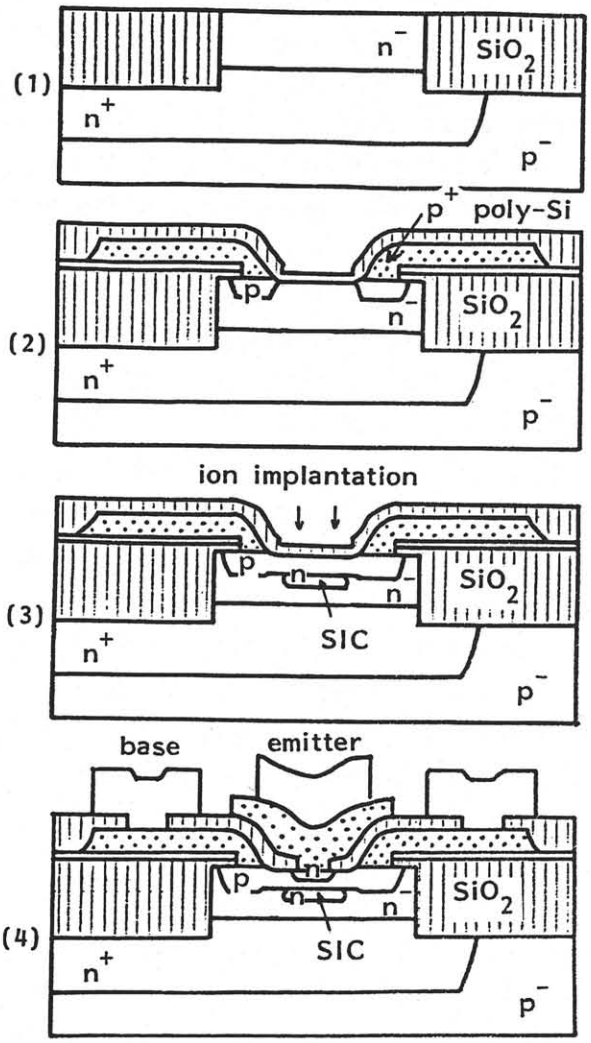

Fig.4 SST-1B process flow.

5. EXPERIMENTAL RESULTS

To evaluate f_{TMAX}, S parameter of test device that 10 transistors were connected in parallel was measured. Each transistor has a 0.35 μm by 13 μm emitter. The measured f_T-I_C (solid curve) at collector-emitter voltages (V_{CE}) of 1 and 3 V are shown in Fig.5. The other f_T-I_C dashed curves are for conventional SST without SIC and with a 1.1 μm epitaxial layer and SPOT isolation.

As shown in the high current range, f_{TMAX} of SST-1B was greatly enhanced to 21.1 GHz (V_{CE} = 1 V) and 25.7 GHz (V_{CE} = 3 V) from 16.8 and 20.2 GHz due to the thinner base width.

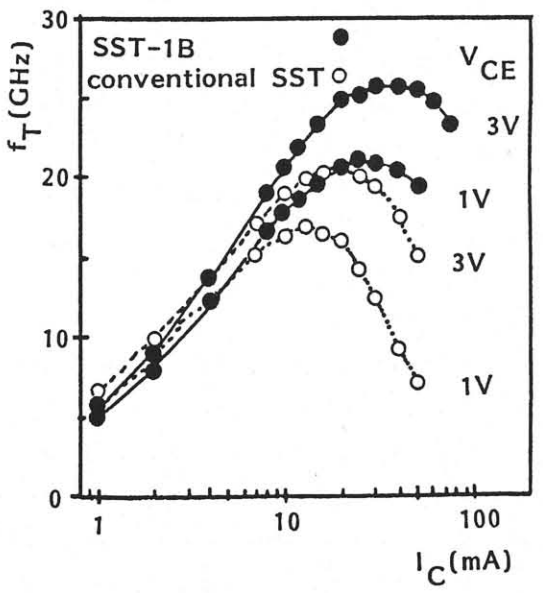

Fig.5 Measured f_T - I_C curves at V_{CE} of 1 V and 3 V for SST-1B (solid) and conventional SST (dashed).

Furthermore, the current density required to attain f_{TMAX} increases by a factor of 2 because of suppression of the pushout owing to the SIC structure.

In the low current range, f_T of SST-1B is a little lower than that of SST without SIC, and the gradient of f_T/I_C is steeper. The main reason for this is that the emitter capacitance of SIC is larger because of a higher base concentration to reduce the intrinsic base resistance.

To measure basic propagation delay, 61-stage NTL and 51-stage ECL ring oscillators (F/I=F/O=1) were fabricated. The logic swing was 450 mV. The measured t_{pd}-power (P) for NTL with a 13 μm-long emitter and ECL with a 7 μm-long one are shown in Fig.6, and are compared with that of conventional SST. The fastest output waveform of the NTL through two-stage emitter follower circuits is shown in Fig.7.

In the low power/current range, the switching delays in NTL and ECL of SST-1B are about the same as that a of conventional SST because of larger intrinsic base-collector capacitance.

Similar to the f_T-I_C result in the high power/current range, the switchings of SST-1B are much faster due to high f_T and low R_{bb}. As a result, minimum delays of 20.5 ps/G (P = 2.32 mW/G) for NTL and 34.1 ps/G (P = 7.54 mW/G) for ECL have been achieved by the advanced SST-1B.

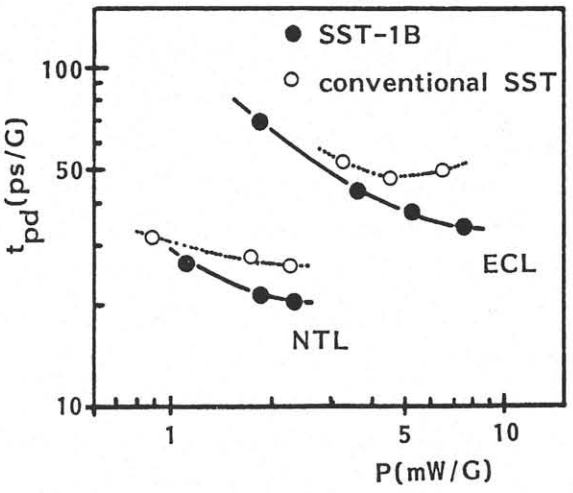

Fig.6 Basic gate delays of NTL and ECL using SST-1B (solid) and conventional SST (dashed).

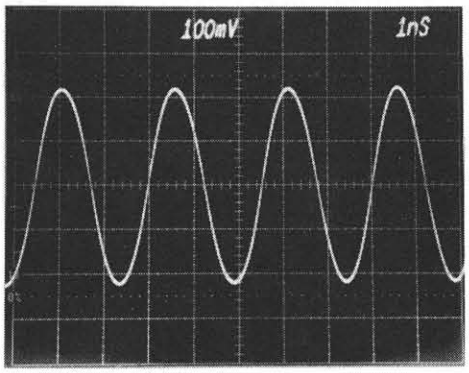

Fig.7 Fastest waveform of 61-stage NTL. The delay time is 20.5 ps/G at 2.32 mW.

6. CONCLUSION

SST-1B with SIC, which is an advanced process to improve a base-collector profile by a selective ion implantation at 150 - 200 KeV, has been developed to increase switching speed. Because SIC can reduce base width and intrinsic base resistance, and can suppress the base pushout effect in SST bipolar transistors, SST-1B has achieved a high cut-off frequency of 21.1 - 25.7 GHz and a fast switching delay of 20.5 ps/G for NTL and 34.1 ps/G for ECL.

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