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Semiconductor Device Simulations for High-Speed Devices

Masaaki Tomizawa, Kiyoyuki Yokoyama, and Akira Yoshii

NTT Electrical Communications Laboratories

3-1 Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-01, Japan

The current status of semiconductor device simulations and new approaches for high-speed devices are described. Attention is mainly focused on the simulation results for various kinds of high-speed devices such as Si MOSFETs, GaAs MESFETs and heterojunction devices. Through these examples, it is demonstrated that the device simulations are important for making accurate performance estimations, even for small devices.

I. INTRODUCTION

In order to realize higher speed and higher integrated VLSIs, devices are becoming smaller and smaller due to the progress in fabrication techniques. With the design of an optimum device structure and confirmation of new ideas for device structure in a short turnaround time, numerical semiconductor device simulation has taken on a significant role in the advance of computational capabilities. Numerical simulations based on drift and diffusion are contributing to actual device design[1]-[10]. For small devices, where nonstationary carrier transport is dominant, simulations based on the Boltzmann transport equation can be performed[11]-[15]. Furthermore, for devices, where quantum size effects are dominant, Schrödinger's equation can be considered for the simulations[16].

II. SIMULATION METHOD

Various device simulation methods are summarized in this secion.

2-1. Conventional model

The conventional model is based upon Poisson's equation and current continuity equations for electrons and holes. These nonlinear partial differential equations are linearlized with Gummel's method[1] or Newton's method[9],[10] and discretized with FDM[9],[10] or FEM[2]. As for the matrix inversion, effective methods such as Stone's[17] and ICCG[18] methods are adopted. The physical models such as field dependent mobility[19],[20] and degeneration[21] are introduced.

2-2. Nonstationary carrier transport model

In small devices, nonstationary carrier transport can play an important role in device modeling. A more accurate model, based on the Boltzmann transport equation is required. There have been two approaches. One is the relaxation time approximation[11],[12], where the carrier transport is calculated by assuming energy dependent relaxation times and the other is particle simulation using the Monte Carlo method[13]-

(15). With this method, the trajectories for all particles in real space and k-space are followed. Furthermore, the electron states in a quantum well, are calculated self-consistently with Poisson's and Schrödinger's equations(16)

III.RESULTS and DISCUSSION

The time dependence of the average electron drift velocity in Si and GaAs is derived under a constant field, as shown in Figs.1(a) and 1(b)(14),(15). From these curves, it can be expected that the nonstationary carrier transport is not as dominant in Si devices, as it is in comparison with GaAs devices. In the following, speed performance for various kinds of devices is estimated using the above mentioned models.

3-1. Si Bipolar Transistor

To improve the switching speed for an npn transistor, thin base thickness to alleviate the base transit time and a thin base-collector depletion layer to reduce the transit time are required. For the device, where the peak of impurity density and width of base are assumed to be $6 \times 10^{18} cm^{-3}$ and 20 nm respectively, the high-speed performance is estimated using a conventional model, as shown in Fig.2.

3-2. Si MOSFET

To estimate the influence of the nonstationary carrier transport, drain currents from the nonstationary models were compared with those from a conventional drift-diffusion model, as shown in Fig.3(22). These features suggest that nonstationary carrier dynamics become dominant for small devices under 0.4 um, even in Si devices. For the device with 2.5nm gate oxide thickness and 0.15 um channel length, the calculated transconductance(g_m) value was 620 mS/mm at 300K(22).

3-3.GaAs MESFET

The nonstationary carrier transport effect becomes dominant in submicrometer gate GaAs MESFETs, as demonstrated in Fig.1(b). The drain currents were derived, as presented in Fig.4(15). It is obvious from this figure that the drain currents obtained by the particle model increase markedly over the drain currents by the conventional model at the submicrometer gate length. This marked increase cannot be obtained in the case of Si. With the gate length reduction, the g_m is greatly improved so that 800mS/mm are estimated with 0.2 um gate length and 45nm eipi-thickness device.

3-4.Heterojunction FET

AlGaAs/GaAs heterostructures such as HEMT(23) have become of major interest due to low-field high mobility. The high mobility of the quantized electron gas can be attributed to reduce ionized impurity scattering due to the spatial separation from the parent donor impurity(24). The device characteristics were calculated using the particle model, as shown in Fig.5. The maximum g_m increased with a reduction in AlGaAs layer thickness, d. This is why the distance between the gate electrode and the electron gas is reduced and the gate controllability can be improved in the same way as in a conventional MOSFET. From the curves, the maximum g_m for L_g=1.2 um and d=42nm device were estimated to be 250 mS/mm at 300K(25). Moreover, for L_g=0.2 um, a g_m value of 400 mS/mm was estimated.

3-5.HBT

High performance was achieved for Si

bipolar transistors with a reduction in geometrical dimensions. The high base concentration to prevent the punchthrough phenomena, however, reduced emitter injection efficiency. An HBT overcomes the above mentioned drawbacks inherent in homogeneous bipolar transistors due to a high injection efficiency owing to wide gap emitter effects. The calculated current gain (h_{FE}) and cut off frequency(f_T) dependence on collector current for the heterojunction- and homojunction-transistors is shown in Fig.6[7]. Moreover, near ballistic electron motion can be counted in the base region. Device performances calculated with the effective ballistic v/E model were also shown in Fig.6. From the figure, the HBT with f_T above 130 GHz and h_{FE} of up to 3200 can be expected.

Performances for high-speed devices are estimated in the above sections. As the further step, it is necessary to take account of total circuit performance and fabrication restriction for the optimization of each device structure in the simulation. Furthermore, it is also important to make the best use of feature in each device for device design.

IV.FUTURE TREND

With regard to VLSI device, the performance of circuits which consist of several devices needs to be evaluated, in addition to each device performance. Thus, hybrid-level models of network equations and the conventional model have been recently developed without a simple equivalent circuit model[26],[27]. This type of simulation will be a powerful tool for the VLSI device design.

Furthermore, deeper theoretical investigation is necessary to more accurately evaluate device performance. For example, two-dimensional electron gas transport properties formed at the AlGaAs/GaAs single quantum wells including multisubband conditions are considered as the step to future accurate device modeling[16].

V.SUMMARY

In this paper, semiconductor device simulation for high-speed devices was reviewed. The rapid progress in computer capability and improvements in numerical techniques have made it possible to widely use two-dimensional simulators, based on drift-diffusion equations. Moreover, for submicron devices, new approaches based on the Boltzmann transport equation have been extensively studied.

Hybrid simulators to analyze the interaction of process, device and circuit will be a powerful tool for the requirement of the total simulation system in the VLSI device design.

For the deeper understanding of device operation mechanisms, device modelings including a further fundamental physics will become increasingly important.

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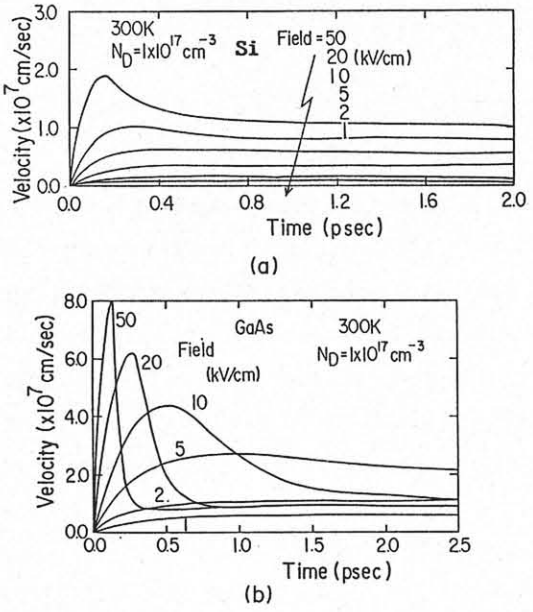

Fig.1 Time dependence of electron drift velocity for (a)Si and (b)GaAs.

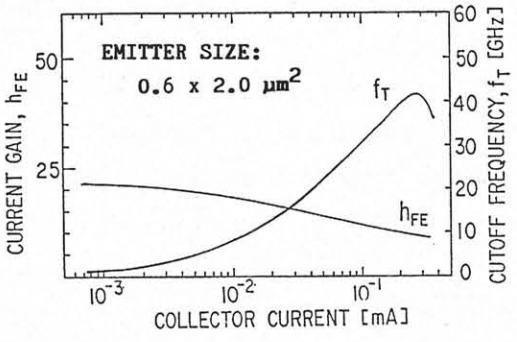

Fig.2 f_T and h_{FE} characteristics versus collector current in Si npn transistor.

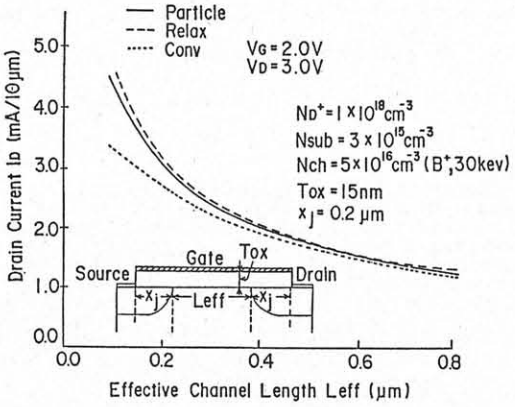

Fig.3 Drain current versus effective channel length for three different approaches in Si MOSFETs.

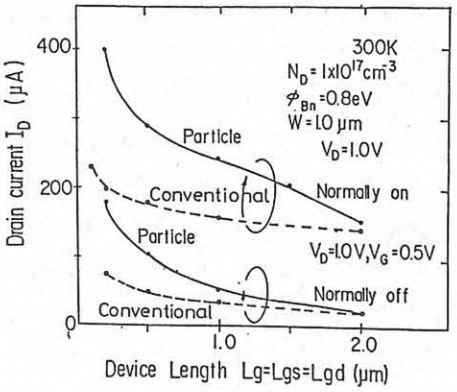

Fig.4 Drain currents versus device length in GaAs MESFETs.

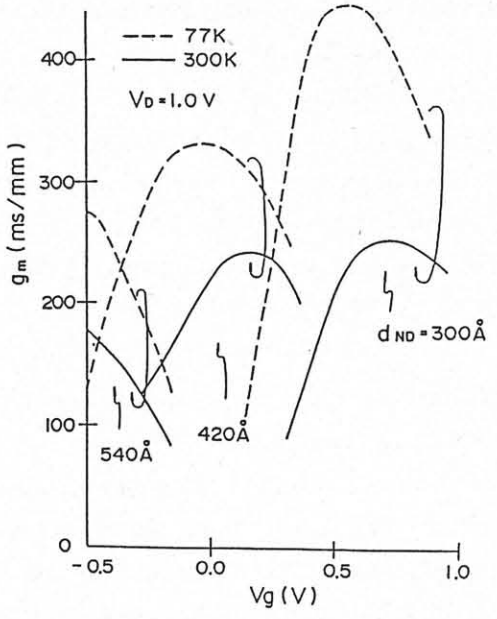

Fig.5 Dependence of g_m on gate lengths in HEMTs.

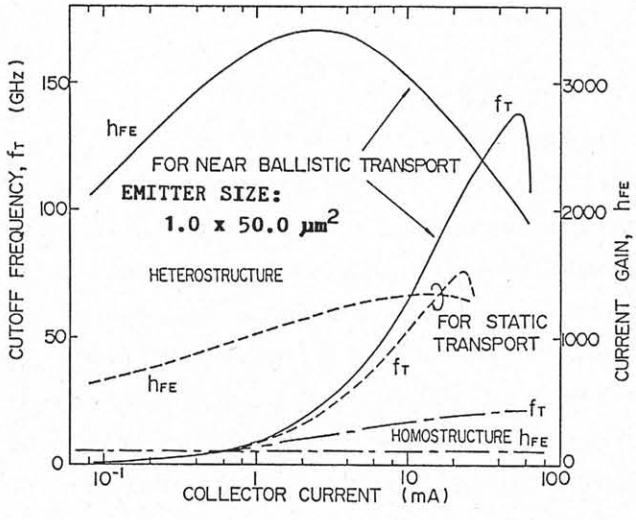

Fig.6 f_T and h_{FE} versus collector current in HBTs.