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Potential of Low Temperature Heterojunction Bipolar IC

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Abstract InAlAs/InGaAs HBTs (Heterojunction Bipolar Transistor) are fabricated and tested. Their dc characteristics are interpreted in terms of tunneling recombination process and hot electron process. The condition for the validity of HBT scaling is discussed. The relation between speed, integration level and heat dissipation at low temperature HBT IC is discussed on the light of HBT scaling rule. Connection of scaled HBT to high Tc superconductor is also discussed.

1 Introduction

As an innovative apporach to the device for future sub ns cycle time supercomputer, a series of work for novel HBT scaling have been published [1]-[3]. In this work, the dc characteristics of InAlAs/InGaAs HBT are studied and the condition for the validity of HBT scaling is dicussed. Then, the relation between speed, integration level and heat dissipation at low temperature HBT IC is discussed. This kind of discussion may arouse some interest since the recent discovery of high temperature superconductors.

2 Current Voltage Characteristics and Tunnelng Recombination

The structure and fabrication sequence of the InAlAs/InGaAs HBT were described before [2], [3]. Figure 1 shows the semi-logarithmic plot of emitter base current as a function emitter base bias voltage. The n values at 77-300 K are nearly unity. This means that the excellent heterojunction are formed. Its n values at 4.2 K are larger than expected, however. This is probably due to tunneling recombination through trapping levels in the junction (Fig.2) [4]. To realize sharp rise in IV characteristics as derived in the 0° K HBT theory[3], these excess recombination current must be eliminated by appropriate device design and processing. This task has not been achieved yet and left for future work.

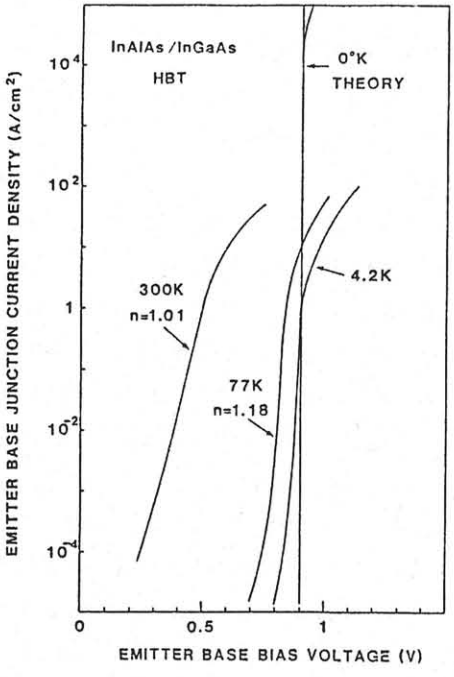

Fig. 1 Temperature dependence of the base current as a function of emitter base bias voltage and its 0°K theory.

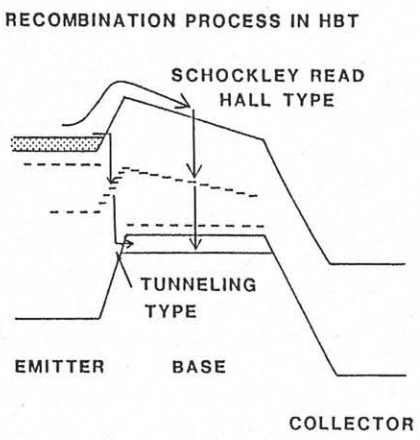

Fig. 2 Minority carrier recombination process in the base regeion of HBT. Tunneling recombination through trapping centers and Schockley Read and Hall recombination process are shown.

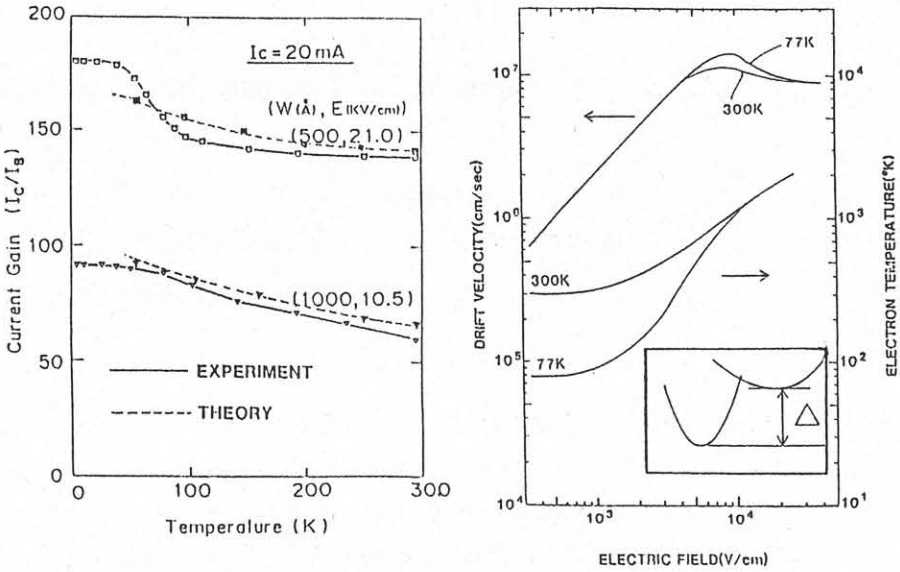

Fig.3(a) Current gain as a function of temperature. (b) Dependence of electron temperature and electron velocity as a function of built in field in the base. $\tau_e = 2\times10^{-12}$, R=94,and Δ=0.5eV. See [5].

3 Hot Electron Effects

Hot electron effects on temperature dependence of current gain

Figure 3(a) shows the temperature dependence of current gain. The base band gap was varied from 0.85 to 0.75 eV over a distance of base width. Strength of built in field ammounts to 10 to 20 kV/cm for 1000-500 A base width samples and electrons injected into base region become hot thereby. In the doping level and temperature range under consideration, dominant recombination mechanisms will be Schockley Read and Hall type one. At the temperature range not too low, nondegenerate statistics for carriers are applicable. In the present model, current gain is a function of eletctron temperature. Electron temperature is calculated as a function of built in field on the basis of the electron transfer model of McCumber and Chynoweth [5]. The agreement between experiment and theory is fairly excellent except the very low temperature range. The dependence of life time on drift field strength is also well understood.

Hot electron effects on IV characteristics

Figure 3(b) shows the calculated electron temperatures rise nearly up to 1000 K. Notwithstanding this, the experimental current voltage characteristics are determined by the lattice temperaures. Theoretically, by considering the electron temperture at the emitter end to be 0° K, the sharp rise in 0° K IV characteristics as obtained in [3] can be rederived [6]. Thus, temperature scaling is valid even at hot electron system and logic swing is scaled down to 0 K in proportion to temperature.

4 Projection of Speed and Integration Level of Scaled HBT

Estimation of low temperature cooling power

In immersed boiling liquid cooling, the maximum heat flux q_{max} carried from the solid surface to the liquid coolant can be estimated as given in TableII.

t_{pd} vs N relation for scaled HBT

Scaling factor of the device is set to the ratio of the boiling point to the room

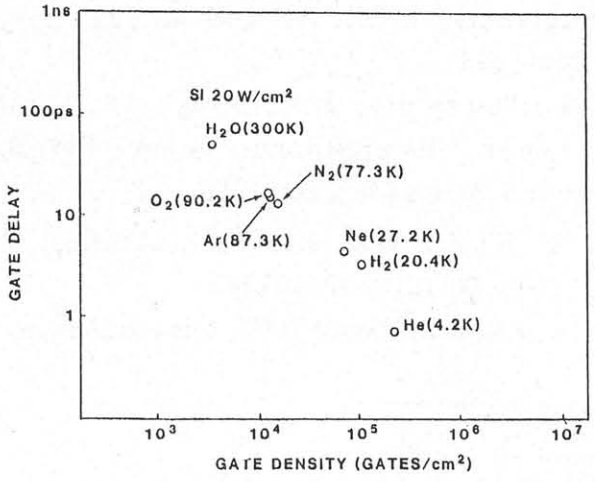

Fig. 4 Propagation delay time vs gate density.

temperature. The parameter of the starting device for scaling is taken from the 1μm x4μm emitter area Si bipolar at room temperature operation [7]. Cooling capability for room temperature Si bipolar is assumed as 20W/cm2. Table II shows propagation delay time t_{pd} and other device parameters scaled from the room temperature Si to those boiling point (B.P.) listed in Table I. From Table II, the maximum gate density N is calculated. The propagarion delay time vs gate density relation thus obtained is shown in Fig.4. It is shown that as compared to Si, an order of magnitude improvement in speed and integration level will be achieved by the low temperature scaled HBT. If the currents are increased by a factor s from the scaled values, the tpd can be reduced from the respective points by the factor 1/s at the cost of the reduction in N by the same factor.

Current density

The problems in current density increase are becoming serious in constant voltage scaling of Si bipolar IC. Table II shows these problems are far more easier for constant field scaling of HBT.

Illustraion of band gap scaling

Design of scaled HBT using various band gap III-V and II-VI compounds is briefly described. Band gap can be continuously varied by using mixed crystal of these semiconductors [8], [9]. From the band parameters, built in voltage, maximum current density J_{max}(at which emitter currents are limited by emitter series resistance), threshold voltage for emitter base junction (defined as the bias voltage at the current level $10-6x\ J_c$) are calculated as shown in Table III. Note that these J_{max} exceed the scaled current density listed in table II. This table clearly demonstrates the superior expected performance of the scaled HBT.

5 Relation to high T_c superconductors

At high current density and low logic swing circuit of scaled HBT circuit, the high Tc superconducting wiring is attractive. Despite the recent rapid rise in Tc and critical current [10], Table III teaches that constant field scaling of HBT should be more attractive than the constant voltage scaling.

As the bias voltage and logic swing of the scaled HBT IC approach to those of Josephson junction circuits with high Tc superconductor, their hybrid circuits may be attractive option for future high performance systems.

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	He	H_2	Ne	N_2	Ar	O_2	water
(°K) B.P.	4.2	20.4	27.2	77.36	87.3	90.2	300*
(W/cm^2) q_{max}	0.482	6.0	7.3	12.6	14.7	15.5	

Table I. Estimation of maximum heat flux.
*operating temp.

	(°K) B.P.	(ps) t_{pd}	(μm) L	(eV) Eg	(V) V_{cc}	(V) δV	(V) V_T	(mA) I_c	(mW) p	(A/cm^2) J_c*	(A/cm^2) J_c**	($gates/cm^2$) N
He	4.2	0.7	0.014	0.02	0.04	0.01	0.008	0.0375	0.0015	4.7×10^6	3.4×10^8	3.3×10^5
H_2	20.4	3.4	0.07	0.07	0.24	0.035	0.054	0.244	0.0586	9.8×10^5	1.37×10^7	1.0×10^5
Ne	27.2	4.5	0.1	0.1	0.32	0.05	0.073	0.244	0.078	7.3×10^5	6.7×10^6	9.3×10^4
N_2	77.36	1.3	0.26	0.26	0.91	0.13	0.20	0.690	0.628	2.6×10^5	9.9×10^5	2×10^4
Ar	87.3	14.6	0.28	0.29	1.0	0.14	0.23	0.779	0.78	2.3×10^5	8.5×10^5	1.9×10^4
O_2	90.2	15	0.29	0.3	1.05	0.15	0.24	0.805	0.81	2.2×10^5	7.9×10^5	1.9×10^4
water	300+	50	1	1	3.5	0.5	0.8	2.68	9.36	6.7×10^4	6.7×10^4	5×10^3

Table II. Device parameters of the scaled HBT. t_{pd}: propagation delay time, L:minimun device dimension, Eg: energy gap, Vcc:bias voltage, δV:logic swing, I_c: collector current, p: power dissipation, J_c: current density. *constant field scaling, **constant voltage scaling N: gate density. +operating temp.

	(eV) Eg	(°K) T	m_c*	m_h*	ε	(cm^{-3}) N_c	(cm^{-3}) N_v	(cm^{-3}) n_i	(V) V_B	(V) V_T	(A/cm^2) J_{max}
InSb	0.17	40	0.014	0.44	17.88	2.2×10^{17}	3.0×10^{18}	1.6×10^7	0.18	0.095	3.8×10^8
InAs	0.356	80	0.023	0.41	14.55	5.5×10^{17}	4.8×10^{18}	1.0×10^7	0.365	0.217	3.8×10^7
GaSb	0.72	200	0.2	0.39	15.69	5.5×10^{18}	9.1×10^{18}	6.2×10^9	0.692	0.385	2.4×10^6
GaAs	1.43	300	0.065	0.47	13.18	2.8×10^{18}	1.4×10^{19}	6.5×10^6	1.39	0.931	3.8×10^6
InP	1.25	300	0.077	0.8	12.35	3.6×10^{18}	2.1×10^{19}	1.4×10^6	1.20	0.76	1.4×10^6
MCT(0.18)	0.028	5			17			6000	0.027	0.017	1.44×10^7
MCT(0.2)	0.066	10			17			21	0.064	0.044	1.44×10^7
MCT(0.22)	0.104	20			17			1×10^5	0.099	0.062	1.44×10^7

Table III. Representative device parameters of HBT and material parameters of III-V binary compound semiconductors. m_c, m_v:effective masses of a conduction and valence band electron, respectively, ε:dielectric constant, N_c, N_v :effective density of states in conduction and valence band respectively, n_i: intrinsic carrier density, V_b: built in field, V_t: threshold voltage for junction current, J_{max}: maximum current defined in the text. MCT(x)=$Hg_{1-x}Cd_xTe$ Donor in emitter and acceptor density in base 10^{19}, 10^{18} cm^{-3} except for MCT's 10^{18}, 10^{17} cm^{-3}.