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A Nanometer-Base Silicon Bipolar Transistor Using an Ultra-Shallow Gallium Diffusion Process

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A new base-forming process using gallium as a p-type dopant was developed. In this process, a shallow and heavily doped base junction is formed by gallium diffusion from gallium-implanted SiO_2 film. The base Gummel number is controlled by ion implantation into the SiO_2 film. For example, a 500Å base junction with a surface concentration of $5 \times 10^{18} cm^{-3}$ can easily be formed with good control. This process is applied for fabricating an NPN planer-type transistor, and the result shows that this process is suitable for forming "nanometer base" bipolar devices.

INTRODUCTION

High speed LSI devices have been achieved with Si bipolar transistors having a very shallow base junction(1),(2) with small lateral dimension. The further reduction of the base width is one of the most important requirements for improving operating speeds. A two-dimensional numerical calculation has shown that the cut-off frequency (f_T) of a bipolar transistor can approach about 40GHz, as shown in Fig.1, if the base width can be reduced less than 400Å.

In a conventional base-forming process using boron ion-implantation, however, it is difficult to reduce the base width below 0.1μm because of base spreading caused by the channeling effect(3),(4). Moreover, although especially high doping is needed in the shallow base structure to obtain low base resistance and high punch-through voltage, the ion-implantation process cannot meet even this demand because crystal damage is unavoidable at high implanting concentrations(5),(6).

This paper proposes a new base-forming process using gallium (Ga) as a dopant. In this process, a shallow and heavily doped base junction is formed in Si by thermal diffusion without crystal damage. In the follwing sections, the process steps and the gallium-diffusion behavior are described. The characteristics of the transistor fabricated by this process will be also shown.

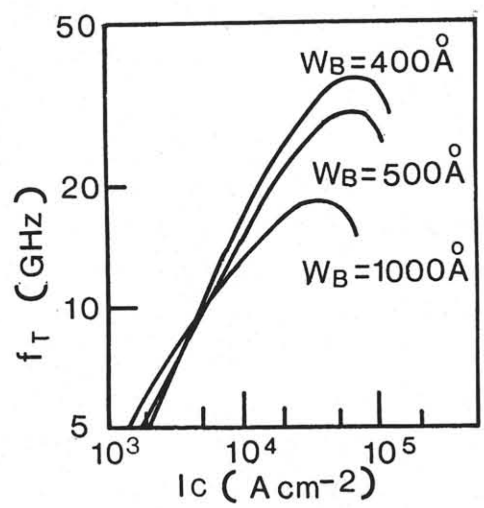

Fig.1 Performance expectation of a Si bipolar transistor.
f_T: cut-off frequency
W_B: base width
I_C: current density

PROCESS

This base-forming process is a combination of ion-implantation and thermal diffusion, and is shown in Fig.2. The process steps are as follows.

(1) A SiO_2 layer and then a Si_3N_4 layer are formed onto a Si substrate. Then gallium is ion-implanted into the SiO_2 layer. (Fig.2-1)

(2) The gallium is introduced into the Si substrate by thermal diffusion from the gallium-implanted SiO_2 layer. (Fig.2-2)

Here, the p-type base junction is formed in the Si substrate. In transistor fabrication, the following step is also performed.

(3) An emitter is formed by arsenic diffusion from an arsenic-implanted polysilicon layer. Then base-contact windows are opened, and Al electrodes are formed. (Fig.2-3)

In this process, gallium is introduced into Si by thermal diffusion, not by ion-implantation, so there is no channeling effect or crystal damage. The gallium diffusion into Si is not significantly influenced by the variability of the SiO_2 film-thickness, since gallium diffusion in SiO_2 is much faster than that in silicon. The total doping quantity, i.e. base Gummel number, is controlled by ion implantation. Thus, a very shallow and highly concentrated gallium base junction is precisely formed.

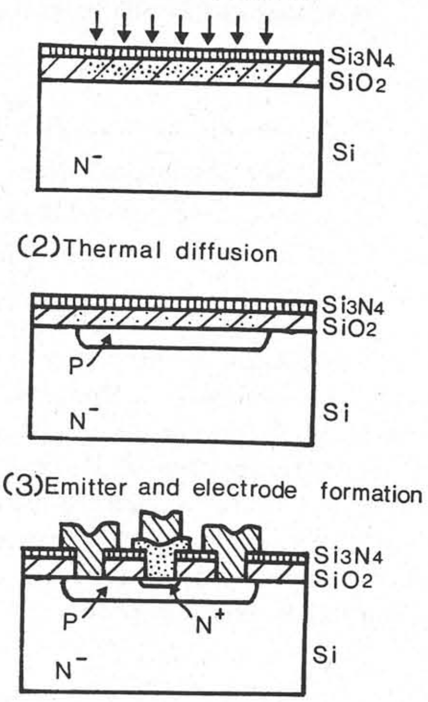

Fig.2 Fabrication steps of gallium base transistor.

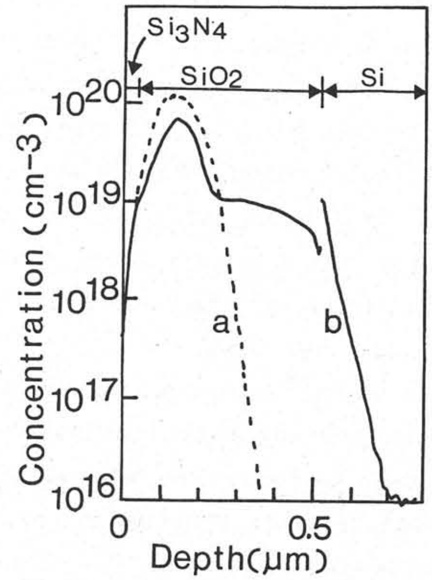

Fig.3 Typical example of gallium diffusion in the $Si_3N_4/SiO_2/Si$ structure.
gallium dose: $1 \times 10^{15} cm^{-2}$, 160keV
Si_3N_4: 300Å, SiO_2: 5000Å
a: Before heat treatment,
b: After 900 ℃-30min heat treatment

EXPERIMENTAL RESULTS AND DISCUSSION

The gallium diffusion behavior in this process was investigated by SIMS method. Figure 3 shows an example of gallium-concentration profile in the $Si_3N_4/SiO_2/Si$ structure after heat treatment. The initial profile of implanted gallium is shown by a dashed line.

It seems that implanted gallium in

SiO_2 seperates into two components: "mobile" gallium and "immobile" gallium. The diffusion coefficient of the mobile gallium in SiO_2 is extremly large, more than 4~6 orders higher than gallium diffusion coefficient in Si. On the other hand, the immobile gallium hardly diffuses at all in SiO_2 even at 1000~1100 °C. The mechanism of this phenomenon is not clear and is now under investigation. The mobile gallium flows so fast in SiO_2 that it immediately reaches the SiO_2/Si interface and diffuses into the Si substrate. At the SiO_2/Si interface, gallium concentrates in the Si side, because the segregation coefficient is greater than one. This favors a heavily doped base layer forming.

Figure 4 shows a gallium diffusion profile in Si at various diffusion times. In this example, a 500Å diffused layer with a concentration of $5 \times 10^{18} cm^{-3}$ is obtained at 900 °C by a 20min heat treatment. The gallium diffusion coefficient in Si was measured at 800~1000 °C, and was found to be slightly larger than that of boron.

Using this process, planer transistors with a gallium doped base were fabricated. Figure 5 shows the current gain h_{FE}, the emitter-collector breakdown voltage V_{CEO} and the emitter-base breakdown voltage V_{EBO} of the fabricated transistors, as functions of gallium dose. The base junction was formed by annealing for 60min at 900 °C. As the gallium dose increases, V_{CEO} increases and h_{FE} and V_{EBO} decrease. This result indicates that the base doping concentration and the base width increase with the gallium implantation dose.

Figure 6 shows the collector current I_C vs. collector-emitter voltage V_{CE} characteristic of the transistor with a $2 \times 10^{14} cm^{-2}$ gallium dose. Current gain of 70~100 was obtained. The Gummel plot in Fig.7 shows that the leak current at the

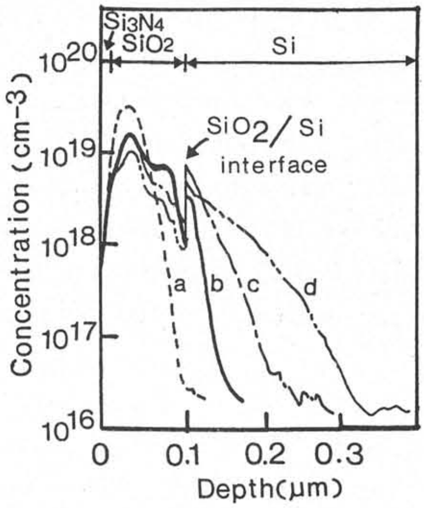

Fig.4 Gallium profiles at 900°C by a:0min, b:20min, c:60min, d:240min heat treatment.
gallium dose: $1 \times 10^{14} cm^{-2}$, 50keV
Si_3N_4: 200Å, SiO_2: 1000Å

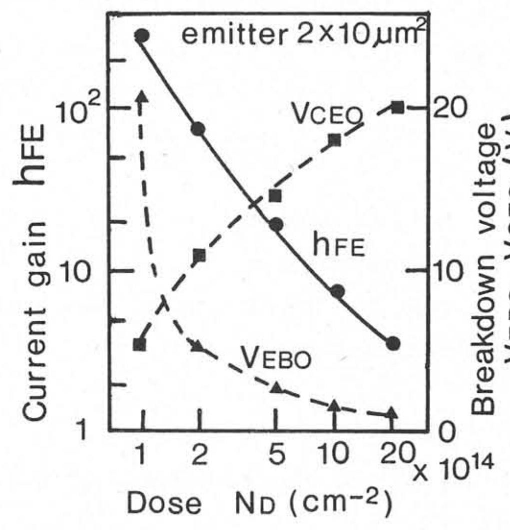

Fig.5 Transistor parameters (h_{FE} and breakdown voltages) for various gallium dose.

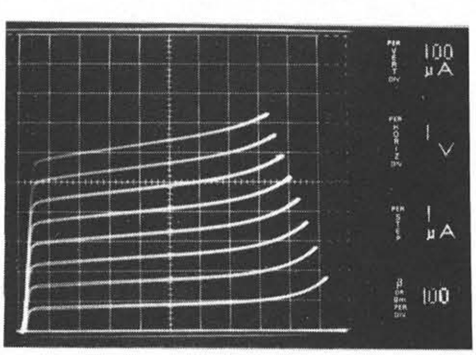

Fig.6 Typical I_C-V_{CE} characteristics (V:100μA/div, H:1V/div, 1μA/step)

junctions is sufficiently low. Figure 8 shows the SIMS-measured doping profiles of the base and the emitter regions. For comparison, ion-implanted boron base profiles with the same base width are also shown. The gallium base has a very sharp profile with a peak concentration several times larger than that of the boron base.

SUMMARY

The new base-forming process using gallium as a dopant was described. In this process, a heavily doped, shallow gallium diffusion layer can be formed without crystal damage. A sharp base profile with a large doping concentration can be obtained, which is impossible in the conventional boron-implanted base. This process is very useful for forming shallow base junctions, and will greatly contribute to the fabrication of high-speed devices.

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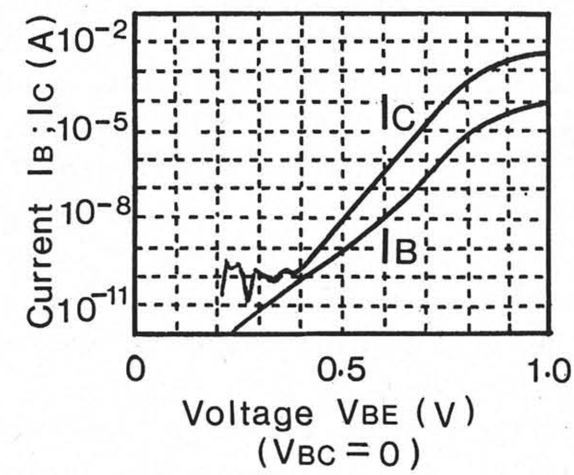

Fig.7 Typical Gummel plot of the transistor.
I_C: collector current
I_B: base current

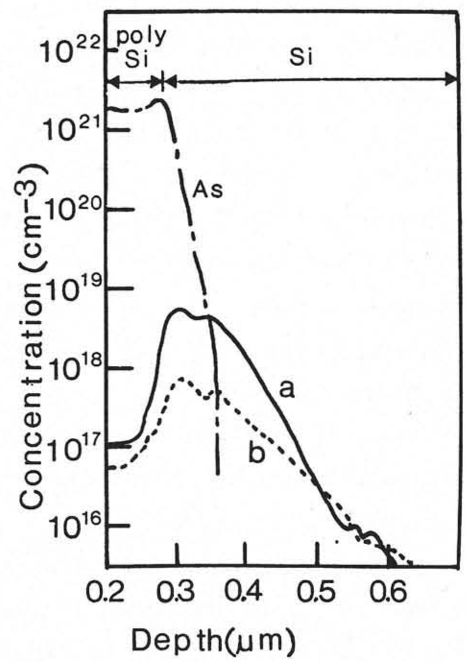

Fig.8Doping profiles of the base and emitter regions.
(a) gallium profile in the gallium base transistor
(b) boron profile in the ion-implanted base transistor.
Arsenic emitter profile is the same for both transistors.