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S-I-4

Device Structure and Electrical Characteristics of SST-CMOS

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A new CMOS process technology has been developed by using SST (Super Self-aligned process Technology) process. Only one photo mask is needed to form transistor active regions including the source, drain junction, and gate. Large transconductance values of 110 mS/mm for the NMOS and 71 mS/mm for the PMOS at V_{DS}, V_{GS}=5 V are obtained. A minimum propagation delay time (fanin = fanout = 1) of 220 psec/gate at V_{DD}=5 V is attained by a 51-stage CMOS ring oscillator.

1. Introduction

Recently CMOS LSIs have been widely used for large integrated memory and logic LSIs, because of low power dissipation. In order to achieve higher logic speed, device size is reduced with an advance of fine pattern lithography or self-aligned technology.

In this paper, a new type of CMOS process, called SST-CMOS, is proposed. A cross section of an SST-CMOS is shown in Fig. 1. This device can be fabricated using a high-speed bipolar SST (Super Self-aligned process Technology) [1] process with only minor modifications. From one gate mask pattern, the dimensions of active areas including gate length, spacing between source and gate and drain and gate, and contact width of source and drain are determined through self-alignment. Therefore, submicron source, drain and gate regions are achievable which will easily lead to high performance CMOS devices.

In the following sections, device structure, fabrication process, basic electrical characteristics, and CMOS inverter characteristics of the newly developed SST-CMOS are presented.

2. Fabrication Process

The main parts of the SST-CMOS process are shown in Fig. 2. The devices were fabricated on (111) p type Si wafers. As well as conventional process, a P well was formed by boron ion implantation into an N^- epitaxial layer after the isolation process.

The SST-CMOS process begins with the Si_3N_4, SiO_2 and undoped poly Si film deposition step. Next, the poly Si is locally oxidized for making poly Si islands. Boron ions are implanted into the poly Si island in preparation for the PMOS poly Si electrode and phosphorus ions are implanted for the NMOS poly Si electrode. The gate window is formed in the poly Si island. During this process, the poly Si island is separated into source and drain electrodes as shown in Fig. 2(a). In the next step, the Si_3N_4 and SiO_2 films on the gate, source and drain contact regions are side-etched through the gate window by means of the SST

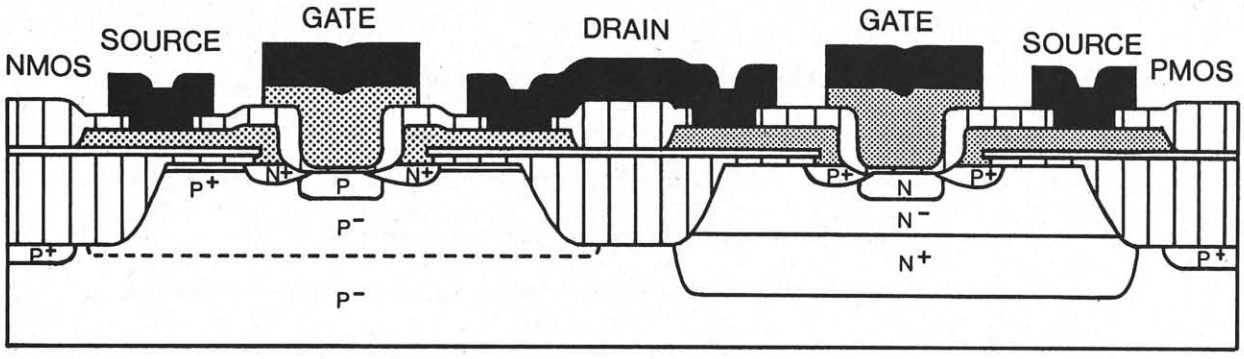

Fig. 1. Cross sectional view of SST-CMOS.

process as shown in Fig. 2(b). The side-etched region under the first poly Si is filled in with undoped poly Si and the unnecessary regions are etched away. The filling poly Si and the substrate of the active region are oxidized. The source and drain areas are formed by diffusion from highly doped poly Si electrodes. Since contact width of the source and drain diffusion area is reduced to 0.3 ~ 0.5 μm, the source and drain junction capacitances can be reduced to less than that of conventional self-aligned MOSs. Channel doping for threshold voltage control is done by ion implantation only in the under-channel region through the gate window as shown in Fig. 2(c). After etching away the SiO_2 in the active region, a 15 nm gate oxide layer is formed. Gate electrodes are formed by arsenic doped poly Si for the NMOS, and boron doped poly Si for the PMOS as shown in Fig. 2(d). The first level wiring, which is 2 μm wide with 1.25 μm spacing, is made of Si-doped aluminum. All metal electrodes contact with highly doped poly Si. Finally, wafers are annealed in H_2 ambience.

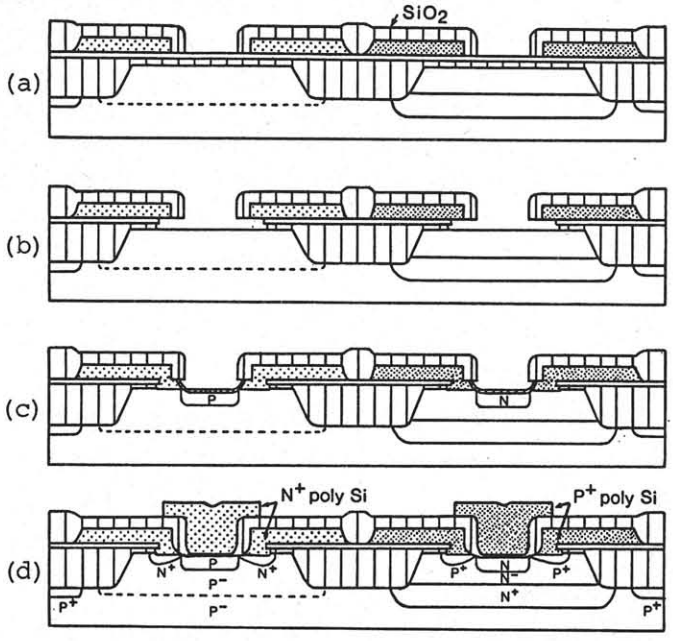

Fig. 2. SST-CMOS fabrication process.

3. Static Device Characteristics

A cross sectional SEM photograph of the PMOS is shown in Fig. 3. From one photo mask pattern, a 1 μm long gate, 0.5 μm source and drain contact width are realized. The I_D-V_D characteristics of the NMOS and PMOS

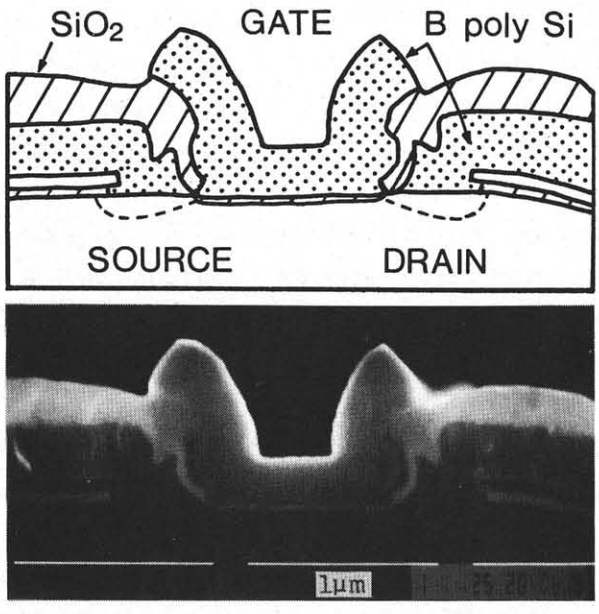

Fig. 3. Cross sectional SEM photograph of SST-PMOS.

devices, both with 1 μm long and 20 μm wide gates, are shown in Fig. 4. The drain breakdown voltage is 5 V for the NMOS and 10 V for the PMOS. Subthreshold factor S at V_{DS}=5 V is 106 mV/decade. This is the same value at V_{DS}=0.1 V for both NMOS and PMOS as shown in Fig. 5. The channel doping method of the SST-CMOS has the additional advantage of making the channel more resistant to punch-through in submicron channel length devices without increasing source and drain junction capacitances. The minimum drain leakage current per gate width is 0.41 pA/μm for the NMOS and 0.76 pA/μm for the PMOS. The maximum transconductance is 110 mS/mm for the NMOS and 71 mS/mm for the PMOS at V_{DS}, V_{GS}=5 V. Threshold voltage, which is controlled by channel doping, is 0.66 V for the NMOS and 0.54 V for the PMOS. The value of threshold voltage was measured from the square root of the drain current versus V_{GS} at V_{DS}=V_{GS}. Threshold voltage dependence on channel length is shown in Fig. 6. The threshold voltage is the same value at a larger channel length over 2 μm, but the value gradually increases as gate length decreases. The similar effect is also discussed for the concave MOS structures[2]. Moreover, it is conjectured that the effect is enhanced by the source and drain junction shape of SST-CMOS which are graded towards the channel region. Source and drain series resistance is 2.95 ohms for the NMOS and 30.9 ohms for the PMOS with a gate width of 200 μm. The PMOS has higher source and drain resistances, because segregation of boron occurs during oxidation. By reducing the source and drain series resistance, a larger transconductance value is expected. Source and drain junction capacitance is 37.5 fF for the NMOS and 20.5 fF for the PMOS with a 0.5 μm long by 20 μm wide junction. Field effect mobility eliminating

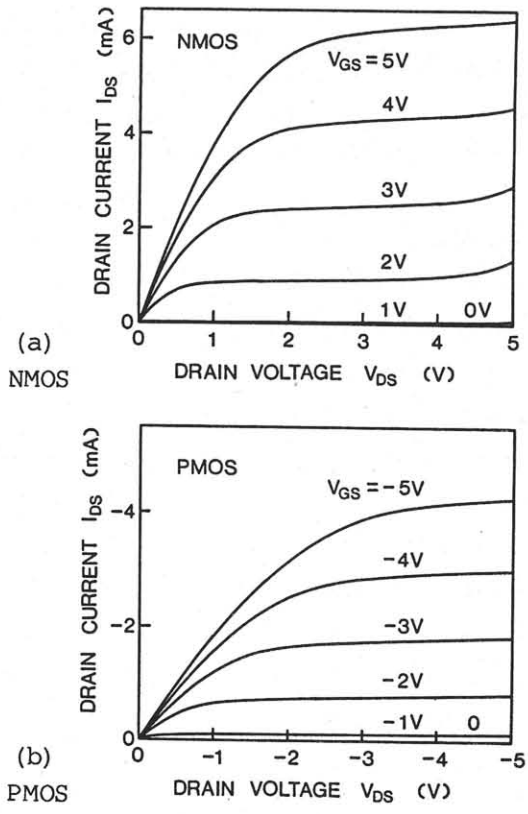

Fig. 4. I_D-V_D characteristics of SST-NMOS (4-a) and PMOS (4-b) with 20 μm wide by 1 μm long gate.

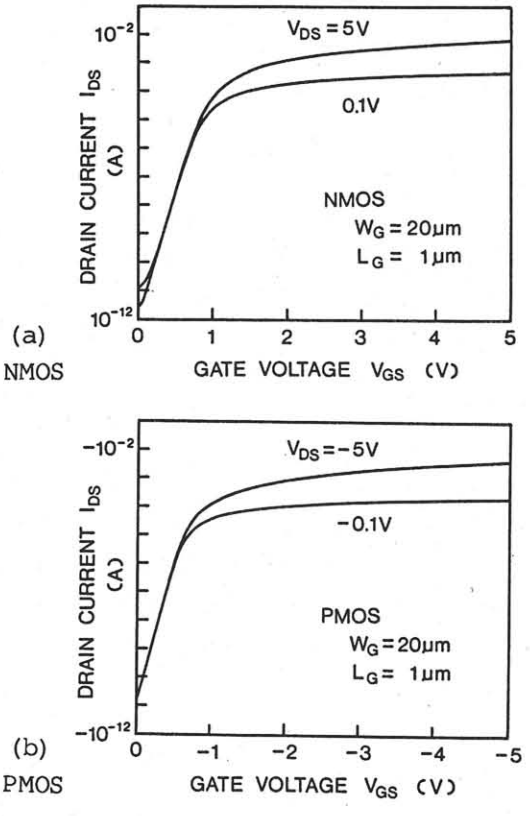

Fig. 5. Subthreshold characteristics of SST-NMOS (5-a) and PMOS (5-b).

the source and drain resistances effect was 354 $cm^2/Vsec$ for the NMOS and 236 $cm^2/Vsec$ for the PMOS with a gate length of 1 μm and a gate width of 200 μm at V_{DS}=0.1 V.

4. Propagation delay time

To evaluate the speed and power performance of these devices, a 51-stage CMOS ring oscillator with an output buffer circuit was fabricated and is shown in Fig. 7. Propagation delay time of the CMOS ring oscillator versus supply voltage is shown in Fig. 8. The minimum delay time of the CMOS with W/L=20 μm / 1 μm for both NMOS and PMOS was 220 psec/gate at V_{DD}=5 V. The output waveform of the CMOS ring oscillator at V_{DD}=5 V is shown in Fig. 9.

5. Summary

A high speed SST-CMOS was developed by using a high-speed bipolar SST process. Large transconductance values of 110 mS/mm for the NMOS and 71 mS/mm for the PMOS and a superior switching time of 220 psec/gate at V_{DD}=5 V was achieved.

Acknowledgment

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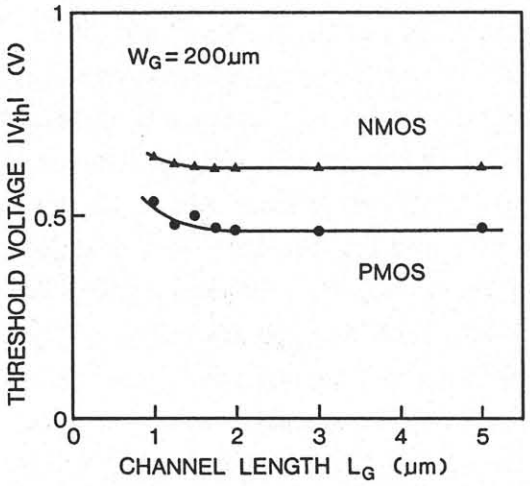


Fig. 6. Threshold voltage dependence on channel length.

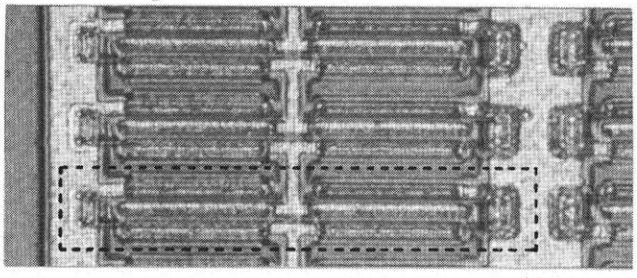


Fig. 7. Photograph of CMOS ring oscillator.

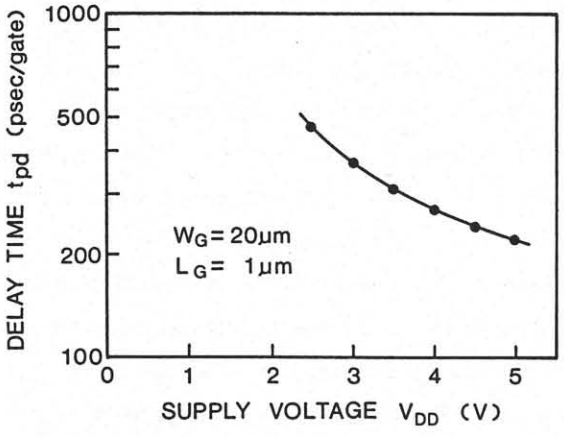
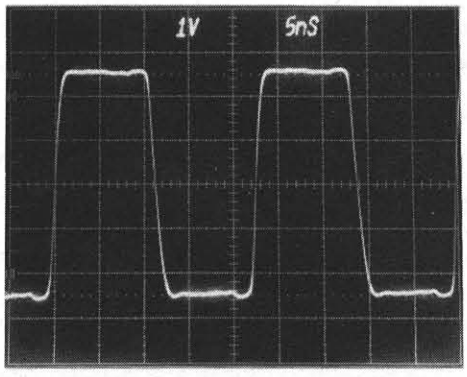


Fig. 8. Propagation delay time of the CMOS ring oscillator.



V: 1V/div.
H: 5ns/div.

Fig. 9. Typical output waveform of the 51-stage CMOS ring oscillator at V_{DD}=5 V.