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Lower Submicrometer MOSFETs Fabricated by Direct EB Lithography

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Lower submicrometer MOSFETs were fabricated by direct EB lithography. They have excellent current-voltage characteristics with high transconductance. Saturation velocity in the inversion layer has been obtained from the channel length dependence of the intrinsic transconductance in the saturated region. The importance of the parasitic resistance has been emphasized from a viewpoint of the device capability in lower submicrometer MOSFETs.

1. INTRODUCTION

VLSI developments require lower submicrometer MOSFETs to achieve higher speed and higher density of the circuits. On the other hand, it is highly attractive for device physicists to fabricate the ultra small transistors and to study the carrier transport in those devices. A few papers report the electrical properties of lower submicrometer MOSFETs by using electron beam lithography [1], or by using the delicate fabrication processes [2]. Recently, NTT group [3] demonstrated the possibility of the extremely high transconductances of lower submicrometer MOSFETs by using ultra thin gate oxides.

In this paper, the device characteristics and physics rather than the fabrication technique are mainly described for the lower submicrometer MOSFETs.

2. DEVICE DESCRIPTION

The devices used in this work were conventional n and p channel MOSFETs fabricated by the direct EB lithography. Both of them have n^+ polysilicon gate. Gate oxides, 5nm and 8 nm, were thermally grown at 900 C in dry oxygen diluted by Ar. The junction depth for n channel MOSFETs is 0.12 μm, though deeper junctions at the contact areas were formed by ion-implanting of As from the contact holes.

3. RESULTS

Figure 1 shows the current-voltage characteristics in the ohmic and saturated region for n and p channel MOSFETs with effective channel lengths of 0.3 μm. Both of them show no evidence of punch-through, though the slight short channel effects are observed in p channel MOSFETs. Subthreshold slope factors, S, at V_D=2 V for n and p channel MOSFETs are 85 and 100 mV/dec, respectively. Figure 2 shows the effective channel length dependence of the inverse of the transconductance, W/gm. C.G.Sodini et al. suggested in Eq.(15) in ref.[4] that the inverse of gm is linearly dependent on the channel length. The experimental results are consistent with the theory. Furthermore, the ultimate value

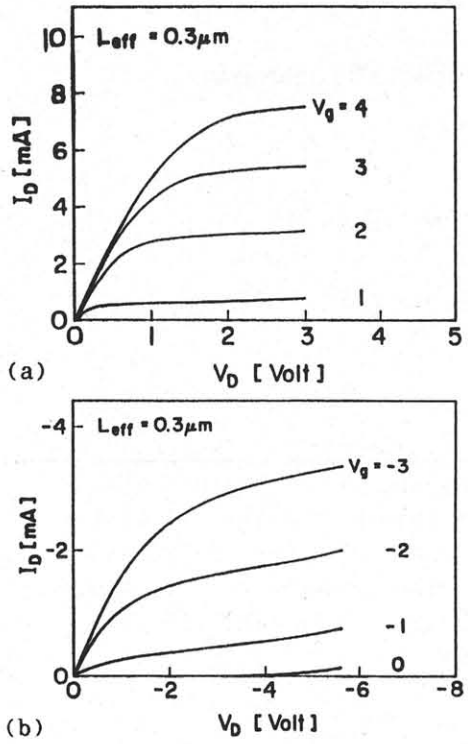

Fig.1 Current-voltage characteristics in ohmic and saturated regions for (a) n channel (b) p channel MOSFETs, with effective channel length of 0.3 μm.

of gm, by extrapolating the line to zero of the channel length, seems to be dependent only on the oxide thickness, regardless of both the channel type and the doping concentration.

The mobility in the linear region is another important subject, both in achieving high speed circuits and in studying device physics in small size devices. Thus, the temperature dependence of the field effect mobility was measured as a parameter of the channel length, as shown in Fig.3. The temperature dependence of the subthreshold slope is also shown. As the channel length decreases, the mobility seems to be less enhanced by decreasing the temperature. Though the applied drain voltage was changed in the linear region, the results were unchanged, as shown for 0.3 μm MOSFET in Fig.3. Therefore, the mobility reduction of the small size MOSFETs at low temperatures cannot be explained only by the hot electron effect

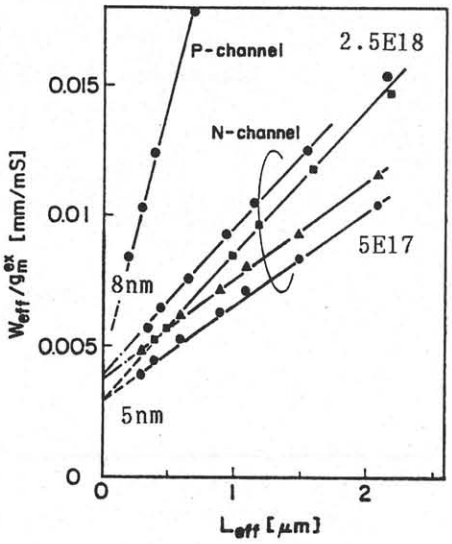

Fig.2 Inverse of the transconductance versus effective channel length of MOSFETs with different oxide thicknesses and with different doping concentrations.

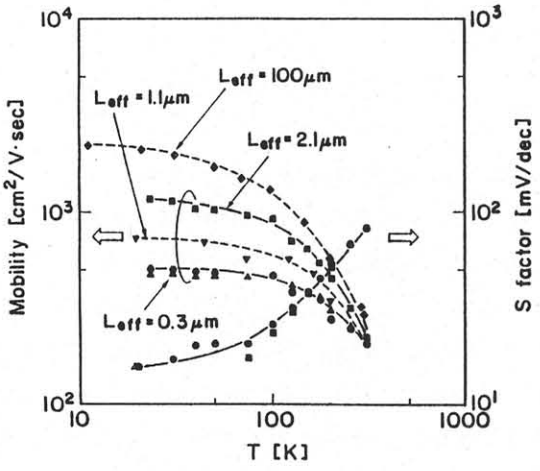

Fig.3 Temperature dependence of the mobility obtained experimentally as a parameter of channel length. The results in two different drain biases are shown for 0.3 μm MOSFET (• ; V_D=10mV, ▲ ; V_D=50mV). Subthreshold slope factors are also shown.

[5].

The substrate current sharply decreases with the gate voltage increase in the case of the long channel MOSFET, while in the short channel MOSFET, the decrease in the substrate current is relatively small. The substrate currents, normalized by the channel currents, are shown in Fig.4 for MOSFETs with various channel lengths. The change of the normalized substrate current with the gate voltage becomes remarkable for the devices with the

channel length of less than 1 μm. In order to clarify the origin of these results, the electric field distributions were calculated by two-carrier device simulator. It was shown that, though the maximum electric field in the channel remains nearly constant even by the channel length reduction, the high electric field region is effectively extended to the channel.

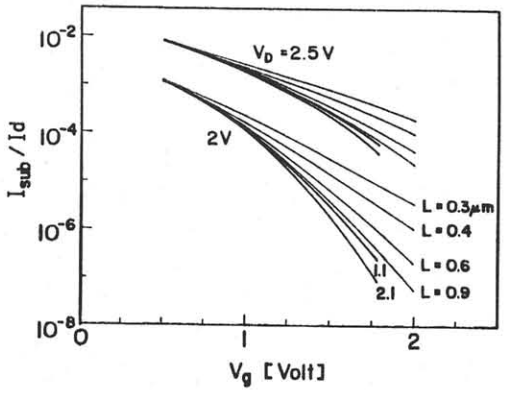

Fig.4 Impact-ionization efficiency versus gate voltage for various channel lengths MOSFETs under two fixed drain voltages.

4. DISCUSSION

In this section, the parasitic resistance effects on the transconductance in the saturated and the linear region are discussed. In the MOSFET with no short channel effect in the saturated region, intrinsic gm, gm^i, can be expressed as follows [6].

$$gm^i = \frac{gm^{ex}}{(1-gm^{ex}*Rs)} \qquad (1)$$

, where gm^{ex} represents gm obtained experimentally and Rs does the parasitic resistance in the source side. Here, devices with the same structure as MOSFETs without gate electrode, as shown in the inset in Fig.5, were used to evaluate the total parasitic resistance, R_T, of the MOSFETs. Figure 5 shows that R_T's in the MOSFETs with the channel width of 10 μm used in this work are 80 ohms for n channel and 60 ohms for p channel, respectively. They can be obtained by extrapolating the lines to zero of Lmask. If Rs is assumed to be a half of R_T, the intrinsic gm can be obtained for the MOSFET with each channel length. The same procedure as in Fig.2 was performed for the intrinsic gm's. Table 1 shows the ultimate values of the intrinsic gm's calculated by the extrapolation. Furthermore, the saturation velocity in the inversion layer can be evaluated by taking accout of the finite inversion layer thickness. In this work, the values of 30 A in n channel and 40 A in p channel MOSFETs were used for the average width of the inversion layer [7]. Recently, MIT group reported the velocity overshoot in the ultra short channel MOSFETs [8], which is the carrier transport phenomenon in non steady state. On the other

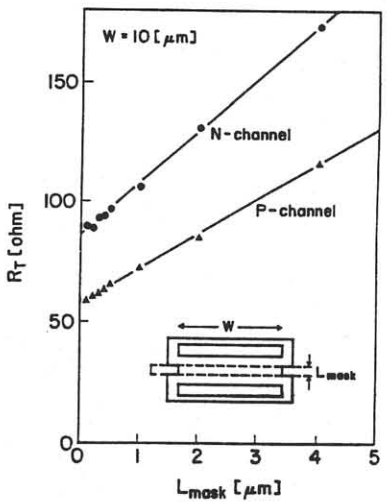

Fig.5 Parasitic resistance versus Lmask, which is shown in the inset. In fact, only diffusion layer exists in the channel.

Channel Type	n				p
T_{ox} nm	5		8		8
$N_A \times 10^{18}/cm^3$	2.5	0.5	2.5	0.5	0.5
g_m^i mS/mm	~380	~430	~330	~340	~260
$V_{sat} \times 10^6$cm/s	7	8	9	9	7

Table 1 Ultimate transconductance values and saturation velocities calculated by Eq.(1).

hand, Table 1 shows the saturation velocity in the inversion layer in a steady state, which is thought to be the first experimental results not influenced by the drain pinch-off effect, except for those by the time of flight technique [9].

In the linear region, gm^{ex} becomes

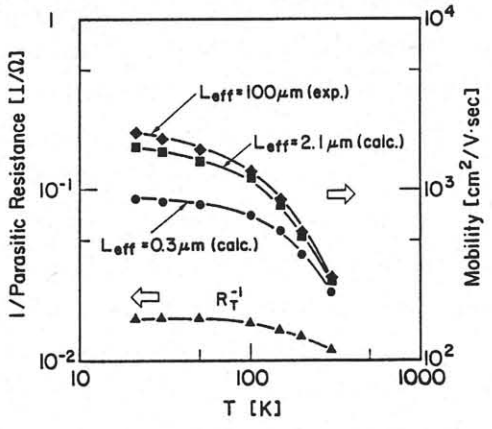

Fig.6 Temperature dependence of the inverse of parasitic resistance. Mobilities calculated by Eq.(2) are also shown, where it is assumed that 100 μm MOSFET has intrinsic mobility.

$$gm^{ex} = \frac{gm^{i}}{(1 + R_T * gd^{i\,2})} \qquad (2).$$

Here, gd^{i} represents the drain conductance. In order to investigate the parasitic resistance effects on the mobility of the MOSFETs with short channel lengths, the temperature dependence of the R_T was measured, as shown in Fig.6. Figure 6 also shows the results of the mobility calculated by Eq.(2). It is clearly shown that the apparent mobility reduction of the short channel MOSFETs at low temperatures is mainly attributed to the effect of the parasitic resistance.

5. SUMMARY

Lower submicrometer MOSFETs were fabricated by direct EB lithography. The transconductances in both the saturated and the linear regions were investigated by taking the parasitic resistance into consideration. The saturation velocity in the inversion layer was obtained from the ultimate value of the intrinsic gm. It becomes more important, for realizing lower submicrometer MOSFETs, to consider the parasitic resistance in the MOSFET in detail.

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