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Substrate Hole Current Generation due to Electron Tunneling in Metal-Oxide-Semiconductor System

A.Toriumi and M.Iwase

VLSI Research Center , Toshiba Corporation

1, Komukai Toshiba-cho, Kawasaki 210

Substrate hole current generation due to tunneling current injection from the inversion layer into the gate oxide has been investigated as a function of gate oxide thickness. It has been demonstrated that there exist three typical mechanisms for the substrate hole current generation depending on the gate oxide thickness. Thinning limit for the oxide thickness has been also discussed.

1. INTRODUCTION

Carrier transport and trapping phenomena in SiO_2 have been studied both intensively and extensively but there are many problems to be clarified from physical points of view. Especially, understanding of the dielectric breakdown mechanism in $SiO_2$is urgently required for realization of future VLSIs. Up to now, there have been many models in which positive charge buildup in the oxide is assumed to lead to the oxide breakdown due to the local electric field enhancement[1]. Other models [2], however, cannot be ruled out. Therefore, it is most important to understand the positive charge generation mechanism due to electron transport in SiO_2.

In this paper, the substrate hole current generated by electron injection to the oxide has been investigated as a function of the oxide thickness. Furthermore, the electron energy in the oxide has been evaluated from the carrier separation experiments.

2. EXPERIMENTAL RESULTS

The devices used in this work were conventional n^+ polysilicon gate MOSFET having various gate oxide thicknesses, all of which were thermally grown in dry oxygen. Substrate hole currents were measured in n channel MOSFETs, while carrier separation experiments were performed in p channel MOSFETs.

Figure 1 shows the experimental arrangement for measuring the substrate hole current in an n channel MOSFET. The gate current Ig, substrate current Isub, and channel current Is were monitored simultaneously.

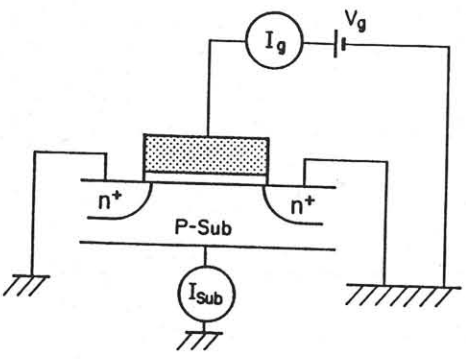

Fig.1 Schematic diagram showing Fowler-Nordheim current injection from Si to SiO_2.

The gate voltage dependences of Ig and Isub in the MOSFET with 112 A gate oxide thickness are shown in Fig.2(a). The ratio of Isub to Ig is also shown. All of them increase with the oxide field. On the other hand, the characteristic behaviors in the ultra thin gate oxide MOSFET are shown in Fig.2(b). Though the gate current increases with the gate voltage, the substrate current and the ratio decrease. Figure 3 shows the ratio of Isub to Ig under two constant gate currents for various gate oxide thicknesses. There are three gate oxide thickness regions (I),(II),(III) for the substrate hole current generation under a fixed cathode field. These results demonstrate that the substrate hole current may be generated not by a single mechanism but by several ones, depending on the oxide thickness or the oxide electric field.

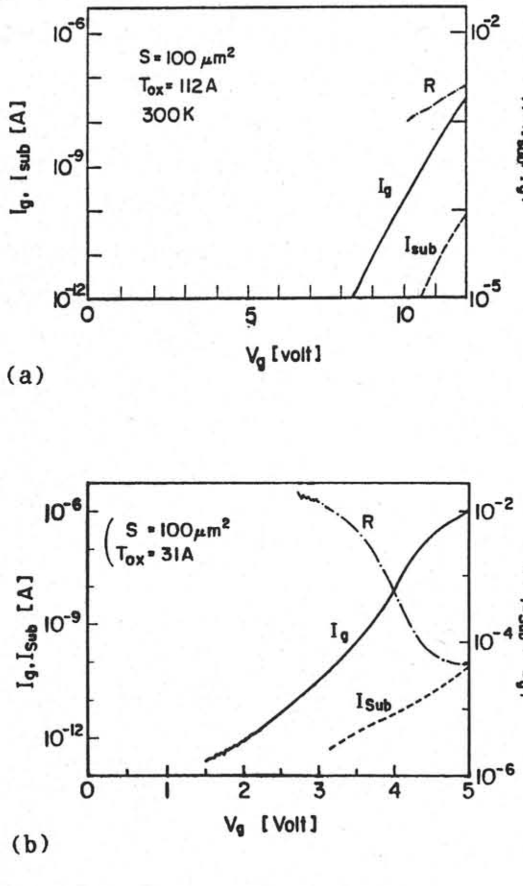

Fig.2 Gate bias dependence of gate current Ig, substrate current Isub and the ratio of Isub to Ig for (a) 112 A oxide thickness, (b) for 31 A oxide thickness.

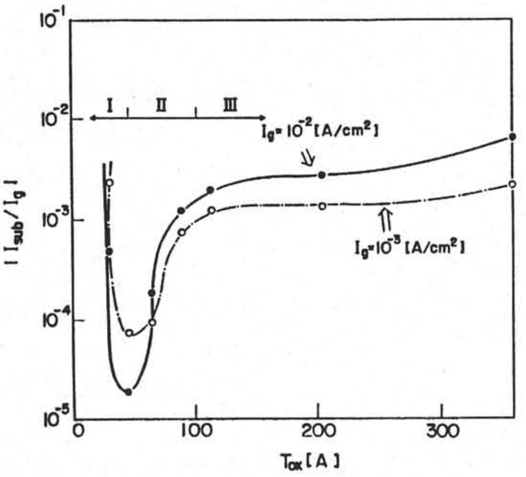

Fig.3 Oxide thickness dependence of the substrate hole current generation efficiency under two fixed gate currents.

Many models for the substrate hole current generation or the positive charge buildup in the oxide have been proposed in the literature [3]-[5]. Basically, three regions exist for the positive charge generation in MOS structure: (a) in the silicon substrate, (b) in the oxide and (c) in the gate electrode. Figure 4 shows the schematic band diagram for the possible mechanisms generating the positive charges. In region (a), valence band electrons are injected into the oxide and the holes left in the substrate can be pushed away from the interface, resulting in the substrate hole current. In region (b), positive charges can be generated by the band-to-band or trap-to-band impact ionization process. In region (c), the impact ionization in the gate polysilicon or photon induced electron-hole pair generation (mediated by surface plasmon polariton [6]) may be related to the positive charge generation.

It is important to know the electron energy in the oxide for discussing the mechanisms mentioned above. Therefore, carrier separation experiments were performed, using p channel MOSFETs [3],[7]. Figure 5 shows the oxide thickness dependence of the quantum efficiency, γ, for impact ionization in the substrate. γ corresponds to the energy of injecting electrons, as calculated by

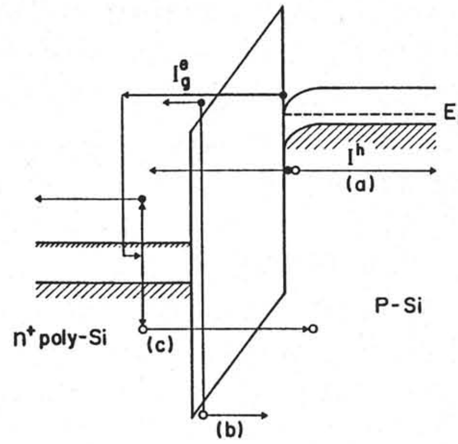

Fig.4 Schematic energy band diagram of MOS structure to show substrate hole current generation mechanisms.

R.C.Alig et al.[8]. From the results in Fig.5, the electron energy in the oxide above 100 A is nearly constant regardress of the oxide thickness, while it decreases with the oxide thickness decrease below 100 A. Thus, the electron energy variation in the oxide is thought to be closely related to the oxide thickness dependence of the substrate hole current. In order to clarify the relationship between them, the results in Fig.3 are shown by linear scale in Fig.6 for the oxides above 40 A. Since any ionization processes should strongly depend on the injecting electron energy, the substrate hole current generation mechanism can be divided into two categories: (i) energy dependent part and (ii) oxide thickness dependent one, as shown in Fig.6.

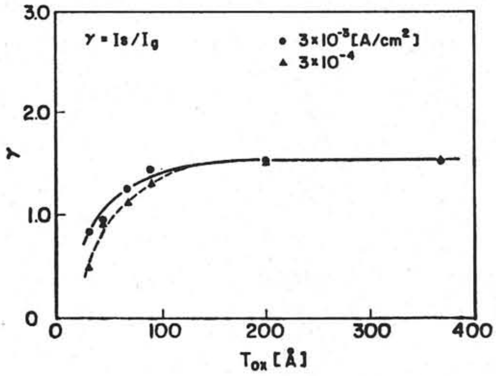

Fig.5 Oxide thickness dependence of quantum efficiency for impact-ionization in silicon under two fixed oxide fields.

4. DISCUSSION

In MOSFETs with oxides thinner than 40 A, the direct tunneling process from the valence band in the substrate to the gate polysilicon is thought to be responsible for the sharp increase with the oxide thickness decrease, since the tunneling of valence electrons should always leave holes in the substrate. In 45 A gate oxide, as shown in Fig.7, the normal Fowler-Nordheim tunneling, which has oscillating component characterizing thin gate oxides [8], is dominant at high electric fields, while the deviation from the Fowler-Nordheim current which shows the direct tunneling, can be observed at low electric fields.

Next, the microscopic origins are discussed for two mechanisms (i) and (ii) in Fig.6. The energy dependent one (i) must be explained by the low energy excitation of holes, because the electron energy gained from the electric field in the oxide is quite low, as compared with the band gap of SiO_2. Though the pair creation in the gate polysilicon or the trap-to-band ionization in SiO_2 can be taken for the substrate hole current, the former is consistent with the results of gate material

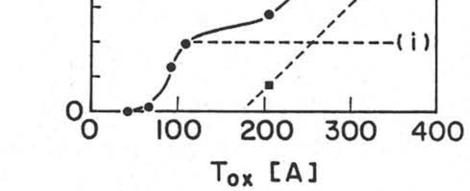

Fig.6 The results in Fig.3 shown by linear scale. Two different mechanisms are shown by dotted lines, which are (i) energy dependent and (ii) oxide thickness dependent, respectively.

dependence at low electric fields [4]. On the other hand, the oxide thickness dependent part is thought to be related to the ionization process in SiO_2, since the running distance in the conduction band in SiO_2 increases and the substrate hole current increases with the oxide thickness.

Finally, the thinning limit for the oxide thickness is discussed. Figure 3 shows that thinner than 100 A gate oxides have smaller substrate hole current generation efficiency. It means the higher oxide reliability in the thinner gate oxides, which has been experimentally obseved [10]. The direct tunneling process in SiO_2 can be, however, clearly observed in thinner than 40 A oxides. Therefore, the intrinsic limit for the oxide thickness will be 30-40 A.

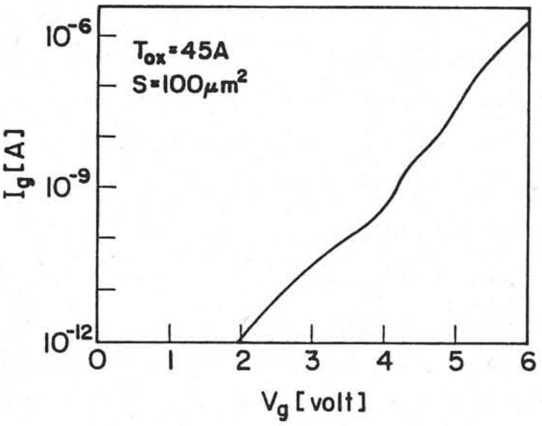

Fig.7 Gate current of the 45 A oxide MOSFET. Both direct tunneling and oscillating regions are shown.

5. SUMMARY

The authors investigated the oxide thickness dependence of the substrate hole current due to the electron injection from the inversion layer into the oxide. It was demonstrated that three typical regions of the substrate hole current generation exist for the oxide thickness variation, depending upon the oxide thickness. They can be explained by the direct tunneling process, the electron hole pair creation in the gate electrode and the ionization process in SiO_2, respectively. Furthermore, the thinning limit for the gate oxide thickness was discussed from the viewpoint of the appearance of the direct tunneling.

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