Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 355-358

Hot Carrier Degradation Masking due to Velocity Saturation in Low Temperature Operated MOSFETs

Kazuo Yano, Masaaki Aoki, and Toshiaki Masuhara

Central Research Laboratory, Hitachi Ltd.

Kokubunji, Tokyo 185, Japan

Hot carrier reliability in submicron NMOSFET at 77K is investigated. A phenomenon called Hot Carrier Degradation Masking is studied in detail, in which the hot carrier degradation of drain current due to DC stress decreases rapidly with increasing the measuring drain voltage. This is observed in single drain and LDD NMOSFETs operated at room and liquid nitrogen temperatures, and is prominent in the forward mode at 77K. The drain current degradation evaluated at the drain voltage $VDMS > 2V$ at 77K is smaller than the degradation at room temperature. A new model based on velocity saturation of electrons explains well the decrease in $\Delta ID/ID0$. Based on this model, the maximum supply voltage for the deep submicron scaled MOSFET is predicted, which shows 77K operation can tolerate even higher supply voltage than 300K operation below $Leff = 0.6\mu m$.

1. INTRODUCTION

Low temperature operation of MOS-VLSI has many advantages 1)2), such as high transconductance, steep subthreshold characteristics, and low wiring resistance. These can realize bipolar level speed and ULSI level integration at the same time. Several authors 3)4), on the other hand, have indicated disadvantages, namely, the enhanced hot carrier generation and the drain current degradation. Von Bruns et al. 5) have pointed out that the degradation decreases as the measuring drain voltage increases in the single drain device. However, the dependence of this degradation on the drain voltage, drain structures and stress conditions has not been fully investigated.

This paper investigates this decrease of the degradation in detail, which we call hot carrier degradation masking. This masking effect is important because it may relieve the hot-carrier immunity problem that is crucial in submicron MOS-VLSIs. Experimental observations in room and liquid nitrogen temperatures, a model using velocity saturation of electrons, and the impact of masking on the maximum supply voltages for deep submicron MOS-ULSIs are also described.

2. EXPERIMENTS

The n-channel MOSFETs measured are fabricated using double well CMOS technology. They have a gate oxide thickness of 25nm and n^+p junction depth of $0.25\mu m$. Two kinds of these MOSFETs are fabricated, one with a conventional single drain and the other with a lightly doped drain (LDD). Moreover, the LDD is formed by either phosphorus or arsenic implantation with an n^- dose of $1 \times 10^{13} cm^{-2}$ at 50KeV and 80KeV, respectively.

These devices were immersed in liquid nitrogen and stressed for 3000 seconds with constant drain voltage V_{Dst} and constant gate voltage V_{Gst}. The electrical characteristics were also measured at 77K before and after stress, with a drain voltage V_{Dms} and a gate voltage V_{Gms}. In addition, identical devices fabricated on the same wafer were also stressed at room temperature, and measured at room and liquid nitrogen temperatures before and after stress. Considering the asymmetry in the device between source and drain produced by the stress, the measurement was conducted in the forward and reverse mode.

3. RESULTS AND ANALYSIS

The degradation rate $\Delta I_D/I_{D0}$ measured in the forward mode is shown in Fig. 1. The stress gate

voltage was set to that which maximizes the substrate current. The rate $\Delta I_D/I_{D0}$ decreases with increase in the measuring drain voltage V_{Dms}, for both the single drain and LDD devices at room and liquid nitrogen temperatures. Note that the rate decreases rapidly for the device measured at 77K, regardless of the stress temperature. Therefore, the degradation rate at a measuring drain voltage larger than 1.2V for single drain and 2V for LDD is smaller at 77K than the rate at room temperature.

In the reverse mode, the degradation rate also decreases with increase in the measuring drain voltage as shown in Fig. 2; however the decrease is smaller than that in the forward mode.

The decrease of $\Delta I_D/I_{D0}$ is also observed for the arsenic-implanted LDD device as shown in Fig. 3(a). In addition, the decrease is again observed when the stress is imposed under the condition that the gate voltage equals the stress drain voltage as shown in Fig. 3(b).

As described above, the degradation-decrease is observed universally for all the devices we measured. The decrease is pronounced in the device operated at liquid nitrogen temperature in the forward mode.

In a previous paper 5), the authors attribute the decrease of $\Delta I_D/I_{D0}$ to the electron-trapping-induced barrier and its lowering due to drain voltage. However, this model does not explain why the $\Delta I_D/I_{D0}$ at 77K in high drain voltage region is smaller than that at room temperature.

A new model including velocity saturation of electrons is given here. In this model, the degradation of drain current is the result of additional coulomb scattering centers produced in the vicinity of the drain, which results in less local mobility of electrons. Although the low-field mobility is lowered by the centers, the saturation velocity v_s is assumed unchanged 6) as follows:

$$v=\frac{\mu_0 E}{1+\frac{\mu_0 E}{v_s}} \quad \text{(before stress)} \quad (1)$$

$$v=\frac{\mu(y)E(y)}{1+\frac{\mu(y)E(y)}{v_s}} \quad \text{(after stress)} \quad (2)$$

where v is the electron velocity, μ_0 and $\mu(y)$ is the low-field mobility before and after stress, respectively, and y denotes the location in the channel. E and $E(y)$ is the electric field parallel to the $Si-SiO_2$ interface before and after stress, respectively. Employing the gradual channel approximation 7), the drain current before and after stress can be obtained. Finally, the degradation rate is expressed analytically as follows:

$$\frac{\Delta I_D}{I_{D0}}=\frac{1}{1+\frac{\mu_0 V_{Dms}}{v_s L_{eff}}}\cdot\frac{\Delta I_D}{I_{D0}}\bigg|_{V_{Dms}\to 0} \quad (3)$$

where L_{eff} is the effective channel length. The calculated results using Eq. (3) are compared with the measured values in Fig. 4. Agreement is good for the device having the channel length of 0.85 μm. In our picture, electrons flowing at the saturation velocity are insensitive to the hot-carrier-induced scattering centers at the drain edge, which causes small change in I_D-V_D curve in the forward mode. In this sense, we call this effect "degradation masking". The masking is pronounced at 77K, because electron velocity is strongly saturated. Note that the shorter the channel length is, the more prominent the decrease of $\Delta I_D/I_{D0}$. $\Delta I_D/I_{D0}$ in high V_{Dms} region directly affects the actual CMOS circuits speed than that in low V_{Dms} region. Therefore, in estimating precisely the hot-carrier immunity of a submicron device and circuit, the masking must be included.

4. ESTIMATION OF MAXIMUM SUPPLY VOLTAGE

Precise prediction of maximum supply voltage for submicron MOSFETs are becoming important, because supply voltage is the key parameter for scaling MOSFETs. In this case, the maximum supply voltage is defined as the maximum drain voltage that can be applied to a MOSFET for ten years without ten percent drain current degradation. Takeda et al. 8) proposed a formula that predicts the maximum supply voltage that is determined by the hot-carrier immunity.

However, this formula neglects the decrease of $\Delta I_D/I_{D0}$ with drain voltage described above. We propose an improved formula including the masking effect as follows:

$$V_{CCMAX}=\frac{1}{B_0+B_1/L_{eff}+(1/\alpha)\ln\tau} \quad (4)$$

where α is a parameter that represents the dependence of $\Delta I_D/I_{D0}$ on stress drain voltage, and the last term in the denominator is the new term representing the masking effect. By using this equation, maximum supply voltage is calculated. The parameters B_0 and τ are determined by the stress experiment shown above, and $B_1(=c_1/\beta)$ is determined by the measured dependence of substrate current on the L_{eff} and V_{Dst} as shown in Fig. 5. The calculated results are shown in Fig. 6. The maximum supply voltage including the masking effect is higher than the voltage without it. especially in the LDD device. In addition, the dependence of V_{CCMAX} on the channel length is small at 77K because of an enhanced masking effect. Therefore, the devices having a channel length smaller than 0.6μm have a higher V_{CCMAX} at 77K than at 300K. This is advantageous for scaling down the device into the deep submicron region at 77K.

5. CONCLUSION

Hot carrier reliability in submicron NMOSFETs at 77K has been investigated. We found that the degradation rate $\Delta I_D/I_{D0}$ decreases considerably with the increase of evaluating drain voltage. This masking effect is explained well by a model that an electron flowing at the saturation velocity is insensitive to hot-carrier-induced scattering centers. In addition, masking effect was found to enhance the maximum supply voltage. Therefore, the masking effect must be considered in precise reliability design for submicron MOSFETs.

ACKNOWLEDGEMENT

The authors wish to thank Dr. Shojiro Asai of Hitachi Central Research Laboratory for valuable discussions. They also would like to express their appreciation to Messrs. Satoshi Meguro and Shuji Ikeda of Hitachi Musashi Works for sample fabrication.

REFERENCES

(1) F. H. Gaensslen, V. L. Rideout, E. J. Walker, and J. J. Walker, IEEE Trans. Electron Devices, ED-24 (1977) 218.

(2) M. Aoki, S. Hanamura, T. Masuhara, and K. Yano, IEEE Trans. Electron Devices, ED-34 (1987) 8.

(3) T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster, and H. N. Yu, IEEE Trans. Electron Devices, ED-26 (1979) 346.

(4) F. C. Hsu and K. Y. Chiu, IEEE Electron Device Letters (1984) 148.

(5) S. L. Von Bruns and R. L. Anderson, IEEE Trans. Electron Devices, ED-34 (1987) 75.

(6) K. K. Thornber, J. Appl. Phys., 51 (1980) 2127.

(7) B. Hoeneissen, and C. A. Mead, IEEE Trans. Electron Devices, ED-19 (1972) 382.

(8) E. Takeda, Y. Ohji, and H. Kume, IEDM 1985 (1985) 60.

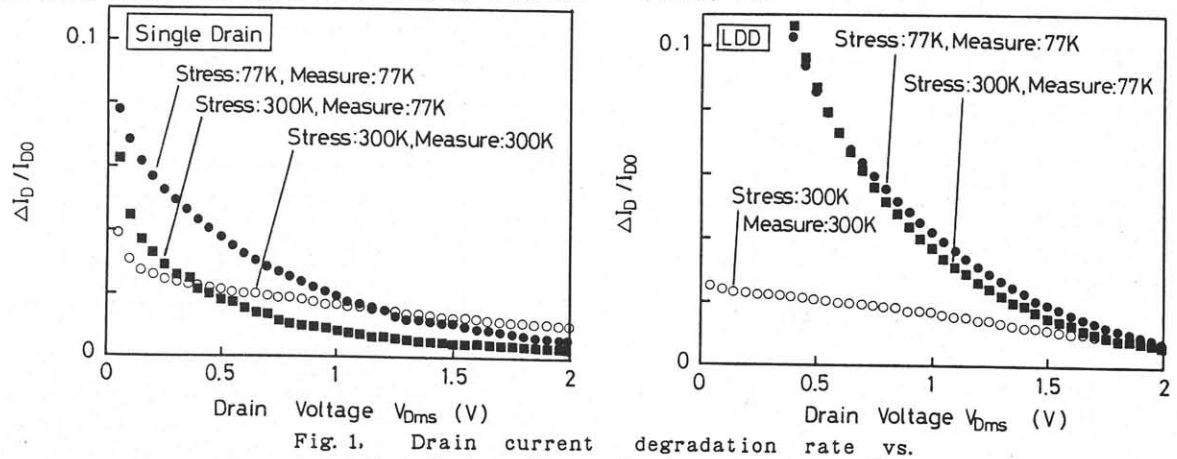

Fig. 1. Drain current degradation rate vs. measuring drain voltage in forward mode. V_{Dst} is 5.5V and 8V for single drain and LDD, respectively. V_{Gst} is such that substrate current is maximum. V_{Gms} is 5V.

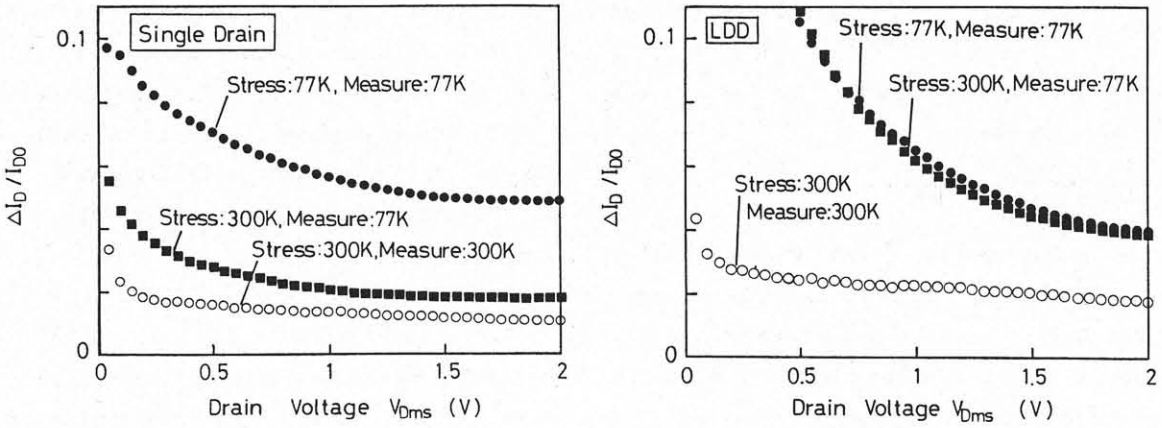

Fig. 2. Drain current degradation rate vs. measuring drain voltage in reverse mode.

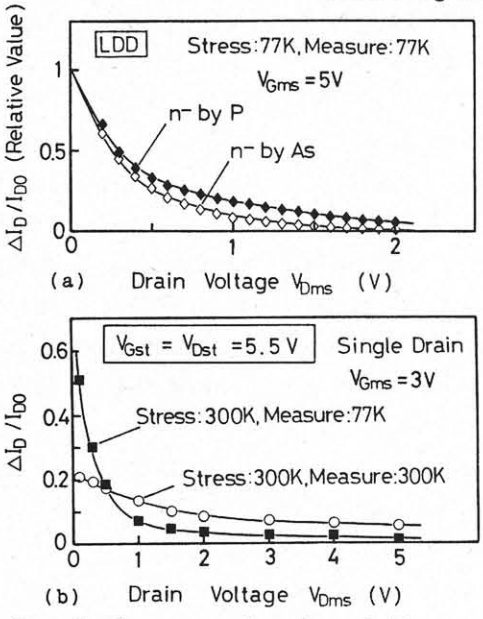

Fig. 3. Drain current degradation rate vs. measuring drain voltage in forward mode. (a):P-implanted and As-implanted LDDs are stressed with V_{Dst} of 8V and 6V, respectively and V_{Gst} is such that substrate current is maximum. (b):single drain device is stressed with V_{Dst} of 5.5V and V_{Gst} of 5.5V.

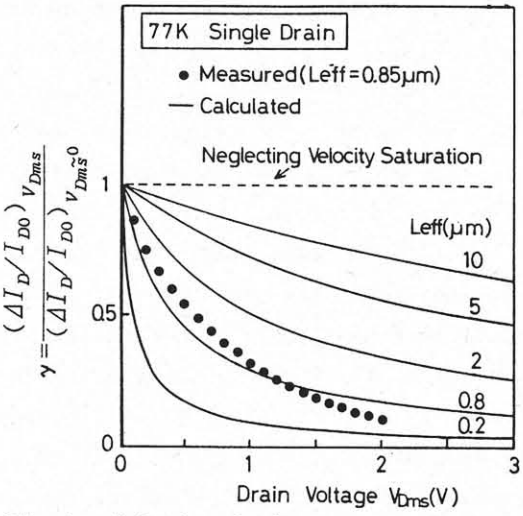

Fig. 4. Relative drain current degradation rate vs. measuring drain voltage.

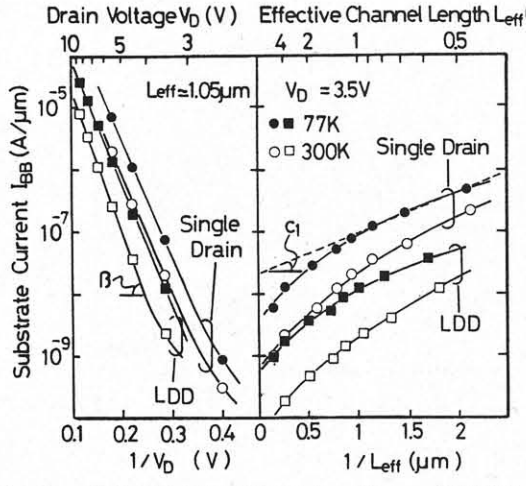

Fig. 5. Substrate current vs. inverse drain voltage and inverse effective channel length.

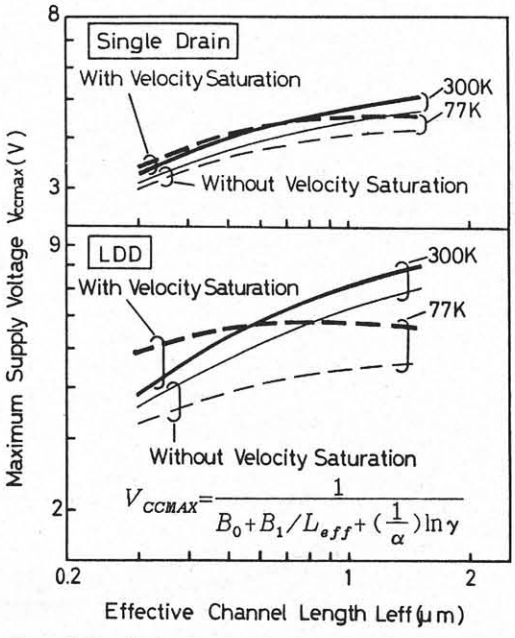

Fig. 6. Calculated maximum supply voltage vs. effective channel length. B_0 is a parameter that represents the immunity depending on the device structure and temperature. $B_1 = c_1/\beta$, $I_{BB} \propto \exp(-\beta/V_{Dst} + c_1/L_{eff})$, α is defined as $\Delta I_D/I_{DO} \propto \exp(-\alpha/V_{Dst})$. $V_{Dms} = 1V$.