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Invited

Recent Advance in Multilevel Interconnection

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The current status of metallization processes is reviewed in this paper. Bias sputter and selective deposition of W and Al are taken as candidates for planarized formation of small via. In view of the fact that few changes is required in the fabrication process, flowage bias sputter seems advantageous. As for the Al alloy component, electromigration resistance of Al-Mg-Si alloy is discussed. Low parasitic capacitance metallization structure for high speed LSIs is fabricated using the contact pillar method.

1. Introduction

For the past 10 years, pattern size of metallization has shrunk continuously each year. Recently, however, as the pattern size approaches 1 or 1.5μm, further shrinkage by the conventional method has become very difficult in terms of both the fabrication process and reliability.

The following are the subjects of current importance.

1) High aspect ratio via contact

Poor coverage of DC sputter metal film results in the disconnection of upper metal mainly at the crossing point over the lower metal and at the via. Troubles at crossing points can be successfully avoided by planarization of insulator films such as with the etch back method. Therefore, disconnection at the via is currently the most serious problem because the ratio of depth/size (aspect ratio) is becoming larger than 1.

2)Component of Al Alloy

Increasing current density requires an Al alloy which is highly resistant to electromigration. In fine Al line patterns less than about 2 μm, disconnection during fabrication, called stress or thermal migration, has become a serious problem. Si precipitation at the contact hole also makes fabrication of small contacts difficult. An improved Al alloy component is required to solve these three problems.

3) Low Resistance and Capacitance.

Parasitic resistance and capacitance accompanied with metallization is also a factor which limits pattern size and device performance. Low resistivity metal, a low dielectric constant insulator and structural improvement are required to solve problem.

This report reviews the current status of metallization by introducing some examples of those newly proposed technology.

2. High Aspect Ratio Via Contact

a. Bias sputter deposition

Planarized deposition by bias sputtering has been achieved by using the re-sputter effect of irradiating Ar ion(Fig.1b). This method successfully planarized Mo, and Al film[1,2]. However, the deposition rate of the re-sputter method is very low for the practical use because about 70 % of deposited metal must be etched to obtain a flat surface[2]. Another problem is the degradation of film quality due to incorporation of Ar ions and damage to the substrate. Film deposited by the re-sputter method usually has a fine grain and high

resistivity. In view of these problems, the re-sputter metal deposition method is not suitable for fabrication.

Recently, a new bias sputter method named Flowage Bias (FB) sputter has been developed[3]. In this method, the substrate temperature is 400 - 450 °C which, in addition to Ar ion irradiation, causes the plastic deformation of Al film to be planarized(Fig.1a). This new planarization mechanism enables formation at 0.5 μm/min. Due to the elevated deposition temperature, only a small amount of Ar is introduced into the growing films and film resistivity is as low as 3 μΩcm. The only difference between this metallization process and the conventional process is that new one is more complicated in detection of alignment marker during lithography. Due to plastic deformation, the grain structure around the via becomes an important factor which affects planarization. Further study is necessary to reveal the effect of grain structure on creep motion. Better uniformity is expected for fine grain films. Optimization of the Al alloy component will improve this method in terms of better control of grain structure, elimination of Si precipitates and Al/Si interdiffusion at contact.

b. Chemical vapor deposition

Recently, application of metal CVD has advanced by utilizing selective deposition of W for plug planarization of vias[4]. W is deposited selectively on Si, silicide and other metals, but not on SiO_2.
The relevant chemical reactions are hydrogen reduction of WF_6:

$$WF_6+3H_2 \longrightarrow W+6HF \qquad (1)$$

and reduction by Si:

$$2WF_6+3Si \longrightarrow 2W+3SiF_4 \qquad (2)$$

Reaction (2) dominates the initial stage of deposition. A selective hydrogen reduction reaction occurs at 300-500 °C. Problems encountered in this method were consumption of Si in the contact area (encroachment) and nucleation on the insulator. Optimization of hydrogen partial pressure and deposition sequences such as 2 step method are required to solve these problems[5].

Chemical vapor deposition of Al film has been studied where mainly various organic metal compounds or $AlCl_3$ are used. Among these deposition sources, tri-isobutyl aluminum (TIBAL) is most popular[6]. In contrast to W, where the reduction reaction is essential, Al is thought to be deposited through two step decomposition of TIBAL:

$$(C_4H_9)_3Al \longrightarrow (C_4H_9)_2AlH + C_4H_8 \qquad (3)$$

and

$$(C_4H_9)_2AlH \longrightarrow Al + 3/2H_2 + 2\,C_4H_8 \qquad (4)$$

Reaction(3) occurs at temperatures as low as 50 °C and forms di-isobutyl aluminum hydride. Al is formed by reaction (4) at about 200 to 250 °C or above. Here, surface preparation with $TiCl_3$ was found to be very important to improve film quality. Nonetheless, film quality such as surface smoothness and reflectivity of CVD Al was far below conventional Al films[6].

Recently, selective deposition of Al films on Si and Al excluding on glass films was reported[7]. Using decomposition of TIBAL, Al was plugged into vias with a 1μm diameter and a 1μm depth as shown in Fig.3. Fig.4 shows that the film thickness increases linearly with deposition time. This results indicates that selective decomposition reaction on the surface occurs. As shown above, Si is not consumed during Al deposition, however, Al/Si interdiffusion cannot be avoided. Therefore, the applications of selective metal deposition are thought to be expanded by using it in combination with barrier layer technology such as TiN.

3. Component of Al Alloy

Electromigration is thought to be a limiting factor in Al metallization. Additionally, disconnection at fine Al lines which is called stress and/or thermal migration has become a serious problem in fine line metallization. This situation has made Al alloy components currently very important.

As for electromigration, Al-Cu Alloy has become popular in fabrication because of improvement in the reactive ion etching process, but Al-Mg alloy also seems to be a candidate[9]. Fig.5 shows that the electromigration resistance of the Al-Mg-Si alloy is comparable to the Al-Cu alloy. In the Al-Mg-Si alloy, Mg is thought to form a

complex with Si (Mg_2Si). In light of this, Si diffusion in Al is suppressed which in turn inhibits the growth of Si nodules at small contact holes.

4. Contact Pillar Method

Fig.6 shows a typical two level structure fabricated using the pillar method. Pillars are initially formed on the 1st metal layer. Next, polyimide films are coated followed by etch-back to expose the pillar top. This method is free from coverage problems and can provide high aspect ratio contact. Fig.7 shows an example of a high speed bipolar LSI fabricated by pillar method. Here, the pillar height is 4 μm with a lateral size of 2x2 μm. Significant reduction in propagation delay (1/2 of that for the conventional structure) was achieved with this structure.

Recently, an advanced pillar method was proposed[10]. Here, as seen in Fig.6a, a polyimide pillar is formed before the 1st metal layer formation. After the 1st metal formation, the polyimide pillar is covered with Al which can connect the two levels. This process results in a very high contact pillar because directional etching by RIE is much easier for polyimide than direct etching of Al. Fig.8 shows the 2 level structure with a pillar height of 10 μm and a lateral polyimide mask size of 1x1 μm. The pillar method is thus thought to be potentially useful for high aspect ratio via contacts.

5. Summary

Some examples of new methods for fine pattern metallization have been reviewed. CVD is expected to be useful for filling high aspect ratio vias, however, further studies on preventing interdiffusion at the contact are needed. The contact pillar process is a candidate for very high aspect ratio contact. In FB sputter method, non-directional incident of Al atoms into vias will limit the applicable aspect ratio. However, as long as the aspect ratio does not exceed much from 1, FB sputter is the most advantageous because almost no change is needed in the fabrication process. As for the Al alloy component, further investigation is necessary regarding barrier layer technology.

6. Acknowledgments

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7. References

1)T. Mogami, M.Morimoto and H.Okabayashi
Ext.Abst.11th Conf.SSDM,Kobe,(1984)p.43
2)Y.Homma and S.Tsunekawa
J.Electrochem.Soc.,132(1985)1466
3)K.Kamoshida,H.Nakamura and T.Amazawa
IEDM Technical Digest(1986)p70
4)T.Moriya,S.Shima,Y.Hazuki,M.Chiba
and M.Kashiwagi
IEDM Technical Digest(1983)p550
5)T.Moriya,K.Yamada.Y.Tsunekawa,S.Nakata
and M.Kashiwagi
Ext.Abst.15th Conf.SSDM,Tokyo(1983)225
6)R.A.Levy,M.L.Green and K.Gallager
J.Electrochem.Soc.,131(1984)2175
7)T.Amazawa, H.Nakamura
Ext.Abst.18th Conf.SSDM,Tokyo(1986)755
8)N.Hara,N.Kobayashi,S.Iwata and N.Yamamoto
Ext.Abst.18th Conf.SSDM,Tokyo(1986)499
9)M.Akiya and H.Nakamura
Tech.Group on SSD,IEICE Japan.
SSD86-172(1987)
10)E.Yamamoto and H.Nakamura
Digest paper, Spring Meeting IEICE Japan. (Tokyo) p2-260 (1987)

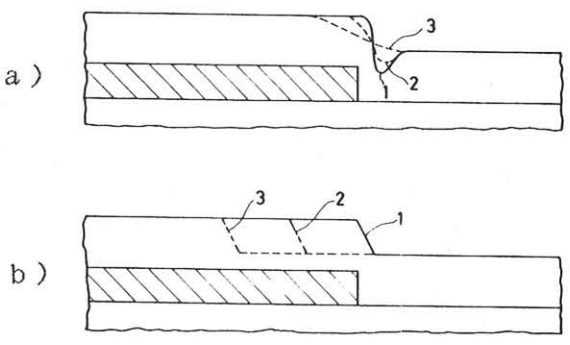

Fig.1 Planarization by bias sputter
a)Flowage Bias (FB) sputter
b)conventional re-sputter

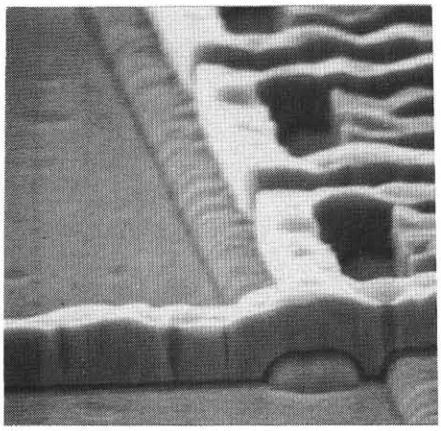

Fig.2 A Planarized interconnection Using FB sputter

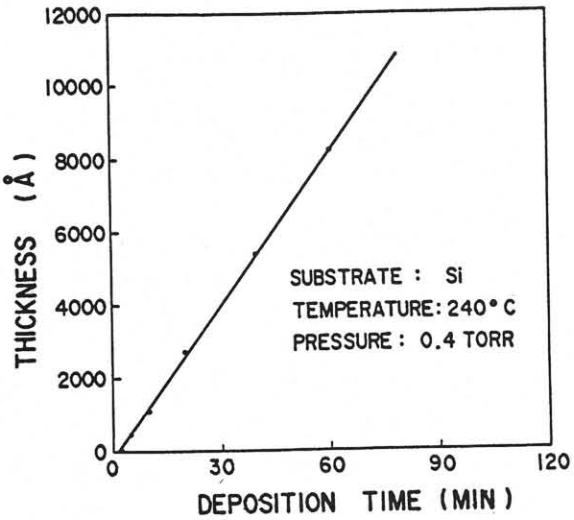

Fig.4 Deposition time dependence of Al film thickness

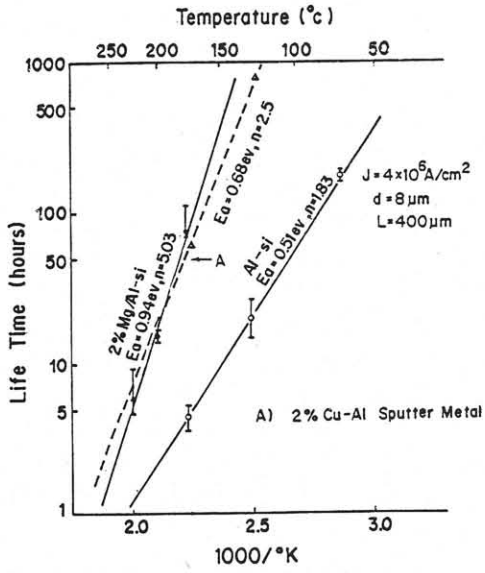

Fig.5 Electromigration failure in Al-Mg-Si alloy film.

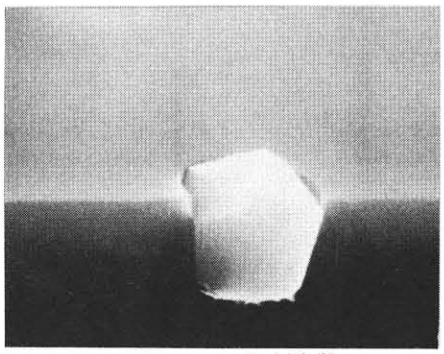

Fig.3 1x1μm contact hole plugged with selectively deposited Al.

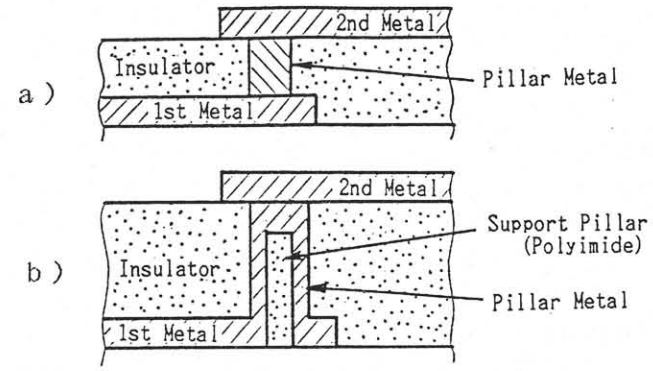

Fig.6 2 level structure fabricated using pillar method.
a) conventional pillar method
b) polyimide pillar method

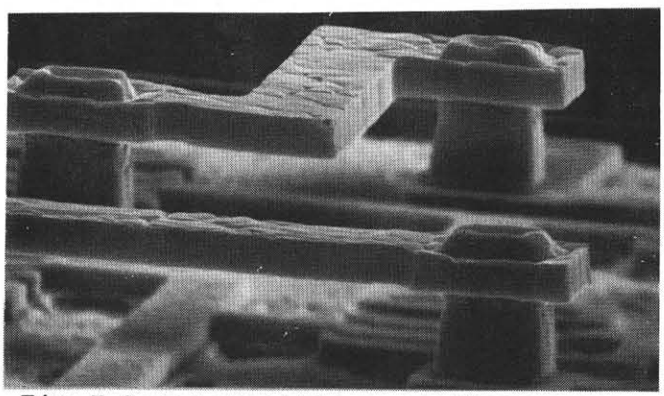

Fig.7 Low parasitic capacitace structure for high speed LSI (polyimide is removed)

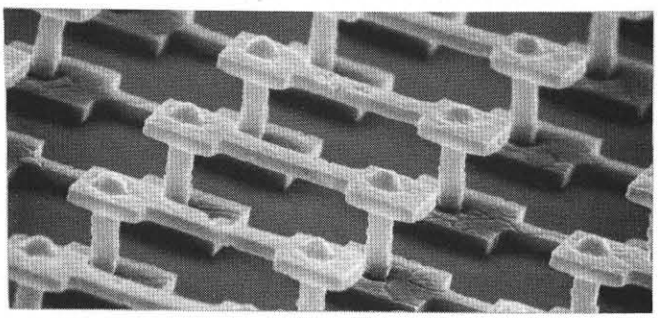

Fig.8 High aspect ratio interlayer connection by polyimide pillar method.(polyimide is removed)