Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, 1987, pp. 443-446

Lift-off Planarization Process for Josephson IC Multilevel Interconnections

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A Josephson IC with 4-level interconnection having less than ~50nm planarity has been fabricated by a lift-off planarization technique. An etching rate difference between films sputtered on a sidewall of the photoresist stencil and on a flat surface was utilized to achieve the smooth lift-off. The high etching rate ratios (100 to 8 for SiO_2 and Nb films) enable tolerant selective etching. After slight etching, residues were eliminated from pattern edge. On the planarized surface, the SiO_2 film with breakdown voltage of 6.3MV/cm, which was 2~3 times as high as that deposited on an irregular surface, was formed.

INTRODUCTION

The very rapid progress in Nb Josephson technology in recent years has extended Josephson devices into ICs such as 16-bit ALU[1] and 3k-gate array[2]. Achievement of Josephson computing systems requires high performance Josephson memory ICs additionally. In comparison with logic circuits, memory circuits are characterized by multilevel interconnection structure because of their electro-magnetically coupling system. To obtain short delay multilevel interconnections, the reduction in the parasitic inductance of the interconnections is essential. Namely, thin insulation layers that allow narrow space between the interconnection lines and the ground-plane are strongly required for high-speed Josephson memory ICs. Particularly in high-density chips, line inductance increase caused by the linewidth reduction must be compensated by the thin insulation layer.

The existence of topographic steps in thin multilevel structure presents several obstacles to the achievement of highly reliable ICs. To heighten the reliability, the planarization process must be applied for the each level in the multilevel structure.

The lift-off planarization technique is used in Josephson memory ICs fabrication process because of its high layer-thickness controlability, low-temperature process ability and pattern-size adaptability.

In the following sections, lift-off planarization procedures, sputtered film properties, planarized layer evaluation and multilevel interconnections for Josephson ICs are described.

LIFT-OFF PLANARIZATION PROCEDURES

The fundamental lift-off planarization process flow consists of 5 basic steps illustrated in Fig. 1. Sputtered Nb and SiO_2 films were used for superconducting layers and insulation layers respectively. Figure 1 shows representatively the case where the patterned Nb film such as interconnections

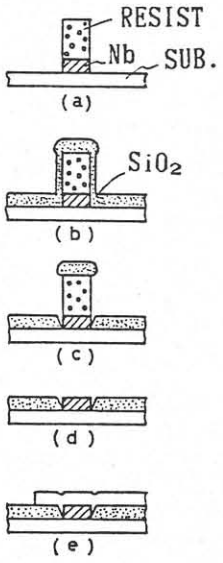


Fig.1 Lift-off planarization procedure, (a) Nb film etching (b) SiO_2 film deposition (c) slight etching (d) lift-off (e) upperlayer deposition

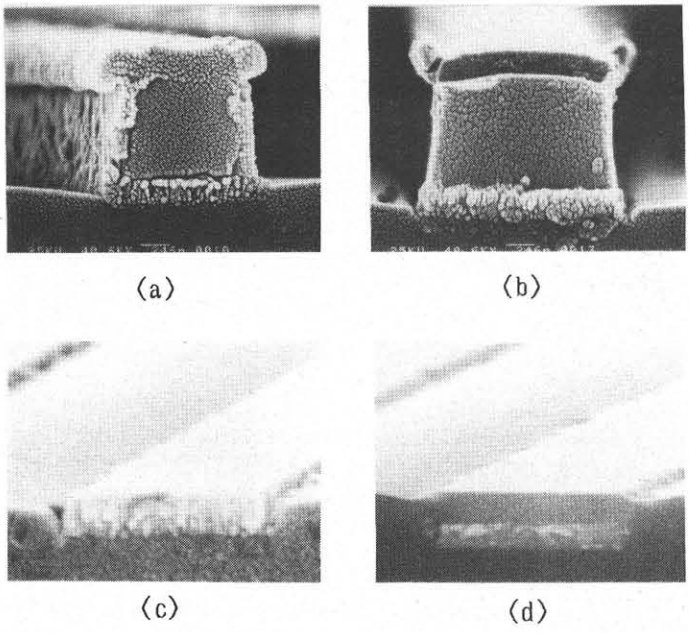


Fig.2 SEMs of the lift-off planarization steps, (a) SiO_2 film deposition (b) slight etching (c) lift-off (d) SiO_2 film deposition

was planarized by the deposited SiO_2 film. The other way, exchanging Nb and SiO_2 each other, the case where the patterned SiO_2 film such as via-hole was planarized by the deposited Nb film was carried out in the same manner.

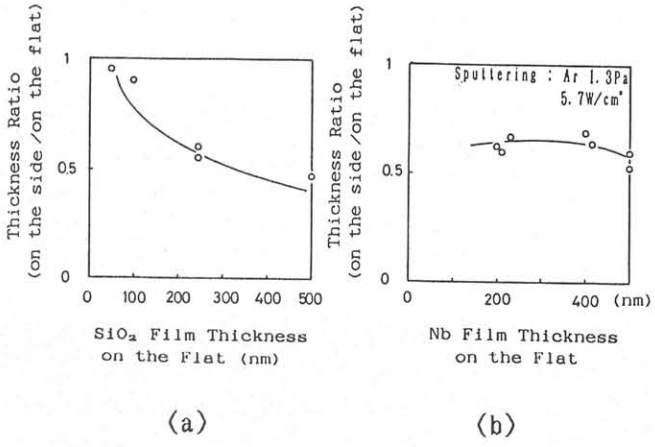
Details of process steps are as follows. (a) A sputtered Nb film is patterned with a resist mask using a reactive ion etching (RIE) technique. Typical etching conditions in a parallel plate system are CF_4 gas of 5 Pa and incident power density of $0.16W/cm^2$. (b) The SiO_2 film is deposited over the entire surface including resist masks under the conditions of 2.2×10^{-1} Pa for Ar and $5.7W/cm^2$ incident power density. The SiO_2 film thickness is the same as the Nb film patterned in the step (a). The sputtered film is also deposited on the sidewall of the etching mask. (c) With SiO_2 slight wet etching, a discontinuity is maintained between the SiO_2 on the substrate and the SiO_2 over the resist mask because the SiO_2 on the sidewall of the etching mask is etched away selectively. (d) During removal of resist in a solvent with an ultrasonic treatment, the SiO_2 film over the resist mask is also removed. Consequently, surfaces of Nb and SiO_2 films which appear in the same level are planarized except grooves. (e) An upperlayer is sputtered over the planarized surface. Finally, the grooves are moderated as described later.

The key step (c) enables smooth lift-off process. Scanning electron micrographs (SEMs) of each step cross sections are shown in Fig. 2.

SPUTTERED FILM PROPERTIES

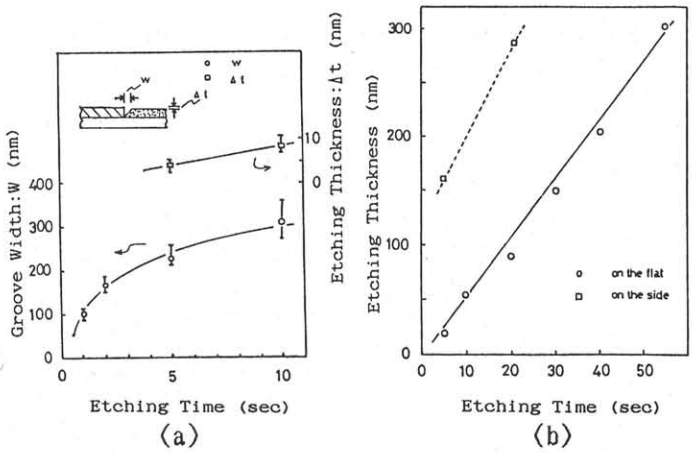
As shown in Fig. 2, the SiO_2 film sputtered over the resist mask was also deposited on the sidewall. Figure 3 shows the thickness dependence of thickness ratio of the film deposited on the sidewall of the step 1.7μm-high to that deposited on the step top.

The SiO_2 film thickness ratio decreases almost exponentially in



(a) (b)

Fig.3 Variation of thickness ratio with film thickness for SiO_2 (a) and Nb (b)



(a) (b)

Fig.4 Selective etching characteristics of a SiO_2 film (a) and a Nb film (b)

increasing film thickness. This result suggests that dominant incident direction of the sputtered particle is perpendicular to the surface. Moreover, a shadowing effect caused by a SiO_2 overhang grown from stencil mask top edge occurs on the sidewall simultaneously. On the other hand, thickness ratio is nearly constant for the Nb film because of a weak shadowing effect.

From the point of view of film quality, the film deposited on the flat surface is constituted by strong coupling layers caused by interfacial mixing. The film deposited on the sidewall is, however, formed by weak coupling particles because of a non-mixing process having a throwing mode only.

Figure 4 shows sputtered film slight etching characteristics at a room temperature. Buffered solutions, HF(1.5mol/ℓ)-NH_4 F(6)-H_2O and HF(1.8)-HNO_3 (4.8)-H_2O are used as etchants for SiO_2 and Nb respectively. The etching film thickness on the sidewall is represented by the groove width because of its measurement ability. The etching rate of the SiO_2 film deposited on the flat was 0.9nm/sec. Thus ~100 of etching rate ratio (SiO_2 deposited on the sidewall to that deposited on the flat) was achieved in 1 sec. etching. For the Nb film, the etching rate ratio is ~8 in 5 sec. etching. Each etching rate difference is evidence of the weak sidewall-deposition-reaction which causes the remaining poor molecule-bonds in the films.

PLANARIZED LAYER EVALUATION

A SiO_2 upperlayer deposited over the grooves moderates their V-shape. The depth and the width of the upperlayer grooves decrease in increasing upperlayer thickness, as shown in Fig. 5. The depth is reduced drastically by the over 200nm thick upperlayer.

Figure 6 shows the distribution of a 200nm thick SiO_2 upperlayer breakdown voltage. On the planarized surface, the SiO_2 film with ~6.3MV/cm of average breakdown voltage which is almost the same as a intrinsic value of the sputtered SiO_2 film was formed. This value was 3 times as high as the SiO_2 film deposited on the non-planarized surface. The most breakdown phenomena occurred at step edges in the non-planarized devices.

MULTILEVEL INTERCONNECTIONS FOR JOSEPHSON ICS

Using the lift-off technique, multilevel interconnections for Josephson

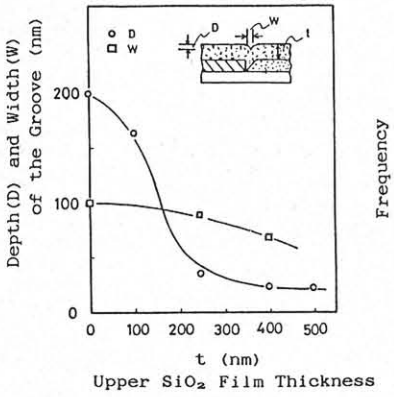


Fig.5 Groove on SiO_2 upperlayer

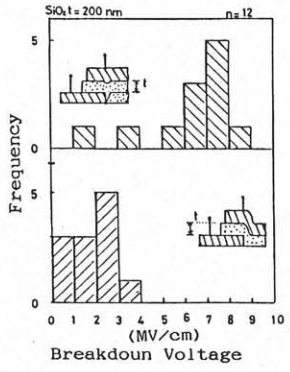


Fig.6 Sputtered SiO_2 film breakdoun voltage

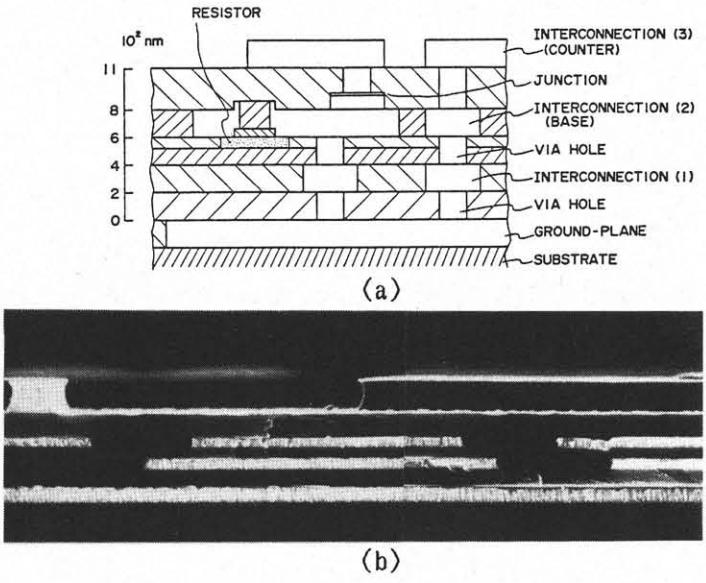


Fig.7 Cross section schema (a) and SEM (b) of VT-NDRO memory cell 4-level interconnection

ICs have been successfully fabricated as shown in Fig. 7. For instance, 4-level interconnections for the high-speed Josephson memory IC using vortex transitional nondestructive read out (VT-NDRO) memory cells[3] consist of a ground-plane, 1st, 2nd (base), and 3rd (counter) interconnections. 200nm thick Nb film was used for these layers. For insulation layer, 200nm thick sputtered SiO_2 film was typically used. When the 200nm thick SiO_2 film was formed on the flat surface, about 165nm thick SiO_2 film was deposited on the sidewall of the stencil mask.

2-second slight etching reduced field SiO_2 thickness by only 1.8nm.

Next to the lift-off process, the 200nm thick SiO_2 film was deposited. As the result, planarized interconnections with less than ~50nm deviation from planarity was fabricated at each level in the 4-level structure.

CONCLUSIONS

A Lift-off planarization technique has been developed and tested for obtaining 4-level interconnections suitable for the high performance Josephson IC. The selective etching which was caused by the slight etching utilizing a high etching rate ratio of the sputtered film between on the sidewall of the resist mask and on the top was achieved. The planarization effect that increases the breakdown voltage of the insulation layer by ~3 folds was confirmed.

ACKNOWLEDGEMENT

The authors would like to thank H. Abe, H. Tsuge, M. Hidaka, S. Nagasawa and J.S. Tsai for helpful discussions and encouragement.

The present research effort is part of the National Research and Development Program on "Scientific Computing System", conducted under a program set by the Agency of Industrial Science and Technology, Ministry of International Trade and Industry.

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