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Silicided Shallow Junction Formation for Scaled-down CMOS Devices

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Rapid thermal annealing and silicidation conditions are discussed to minimize the leakage current of shallow implanted junctions for sub-μm CMOS devices. A relatively low cooling rate of ~7°C/s as well as $TiSi_2$ formation after implantation/annealing have been found to be preferable to reduce the leakage current at the junction perimeter down to $\sim 2\times10^{-16}$ A/μm at a reverse bias of 5V. This is because increase in the surface recombination velocity or defect generation induced by stress at the perimeter can be avoided under the above condition. In addition, characteristics of MOSFET's are demonstrated with emphasis on the effects of a silicided source/drain thus formed.

1. Introduction

With the scale-down of CMOS devices, shallower and low resistivity source/drain junctions are required to maintain low junction leakage current. Shallow junctions have been obtained by effectively reducing the annealing temperature of the implanted layer. Rapid thermal annealing (RTA) technology is a very promising candidate for this reduction; however, thermal stress of RTA affects the leakage current at the perimeter of the junction[1]. On the other hand, low resistivity junctions have been obtained by a silicided layer. For example, $TiSi_2$ layer decreases sheet resistance by more than one order of magnitude as does conventional As doped layer[2]. In addition, scaled-down junctions, with an area of less than 1 μm^2, are required to reduce the perimeter leakage, because the perimeter-to-area ratio becomes larger as devices are scaled.

This paper describes a suitable process technology for the formation of source/drain regions, with shallow, low resistivity and low leakage current characteristics. Increase in leakage current due to low temperature annealing, RTA thermal stress and $TiSi_2$ formation are quantitatively discussed.

2. Experimental Procedures

A p-type, (100)oriented, 10 Ω-cm Si substrate was formed with p-type and n-type well layers. Device isolation was performed by LOCOS with a p-type channel-stop layer. Ion implantation and annealing technology were used to fabricate n^+ and p^+ layers, as shown in Table 1. Conventional furnace annealing (FA) and RTA were utilized with controlled heating and cooling rates of about 4-50°C/sec above 600°C.

A $TiSi_2$ layer was formed by a self-aligned process utilizing RTA in N_2[3]. An n^+ or p^+ junction is formed before or after $TiSi_2$ formation, as shown in Fig. 1. Further, annealing after $TiSi_2$ formation decreased the contact resistance between doped layer and $TiSi_2$[3].

The surface recombination velocity (S_0) was obtained from the relationship between

leakage current and the area of surface depletion region[4], measured on a gate controlled diode, as shown in Fig. 2.

3. Results and Discussions

Junction formation conditions, junction depth (x_j) and leakage current of the 5V reverse biased n^+/p junctions are shown in Table 2, where area component (J_a) and perimeter component (J_p) of the leakage current are indicated separately. These results are summarized as follows.

(1) J_a is small for junctions treated with long annealing time and having large redistribution of implanted As, as in results 1, 2 and 3. However, J_p hardly depends on the above conditions.

(2) J_p is large for RTA with rapid heating and cooling, as in results 1 and 4. And J_p is small for RTA with slow heating and cooling, as in results 4, 5 and 6. In particular, the effects of the cooling rate is large. Furthermore, J_a hardly depends on the heating and cooling rate at RTA.

Annealing conditions, x_j and leakage current of the -5V reverse biased p^+/n junctions are shown in Table 3. In the p^+/n junction, J_a is also small for large redistribution of implanted B, and J_p is small for a low heating and cooling rate. These experimental results clearly indicate that the cooling rate, rather than the heating rate, affects the leakage current and that J_p rather than J_a affects the total leakage current.

The relationship between J_p and S_0 was obtained on various junction formation conditions, as shown in Fig. 4. The extent of J_p depends almost linearly on the amount of S_o, which is attributed to deep trap levels due to thermal stress[5]. Therefore, in scaled devices, the control of deep interface traps is most essential to decrease the leakage current level.

Next, the results of $TiSi_2$ formation are described. The sheet resistance was decreased to 3~5Ω/□, and the x_j of n^+/p junction and p^+/n junction were about 180nm and 300nm, respectively. The dependency of J_a and J_p at V_r=5V on process conditions is shown in Fig. 3, where it is depicted that J_a and J_p did not increase if the $TiSi_2$ layer is formed after the n^+ or p^+ doped layer. This phenomenon is attributed to the increase in junction depth (x_j) by $TiSi_2$ formation as shown in Table 2. On the other hand, J_p and J_a increase when the n^+ or p^+ doped layer is formed after $TiSi_2$ layer formation. The increase in J_p at the n^+/p junction is especially attributed to the $TiSi_2$ stress effect[6].

These experimental results indicate that J_a is affected by redistribution of implanted dopant, and that J_p is controlled by the stress induced surface state during annealing of the implanted layer.

MOS transistor characteristics fabricated by optimized process conditions are shown in Table 4. The drain breakdown voltage (BV_{ds}) was improved, and the ratio between drain current and substrate current (I_{sub}/I_d) was reduced by an optimum process sequence, which forms an n^+ or p^+ region after self-align $TiSi_2$ formation. On the other hand, decrease of I_{sub}/I_d and increase of mutual conductance (g_m) were obtained by $TiSi_2$ formation on an doped layer. These results are attributed to the decrease in leakage current and resistivity by $TiSi_2$ formation. The shift of gate length (ΔL) was in proportion to x_j, and is decreased with a decrease in x_j. RTA was effective in improving the p-channel device, for example, by increasing BV_{ds} or decreasing ΔL and I_{sub}/I_d.

4. Conclusion

The perimeter component leakage current which is important for a scaled-down junction, was found to be controlled by stress during annealing of the implanted layer. Moreover, for realization of titanium silicided shallow junction formation with low leakage, it was clarified that an n^+ or p^+ doped layer with good leakage current characteristics should be formed before $TiSi_2$ formation. The above effect was confirmed by a sub-μm MOS device characteristics.

Reference

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Table 1 Conditions of junction formations.

		n^+/p junction	p^+/n junction
implantation		As^+, 40keV and 80keV, $5\times10^{15}/cm^2$	B^+, 10~15keV, $2\sim3\times10^{15}/cm^2$
annealing	FA	950℃, 10min. (+900℃, 15min.)	900℃, 15min.
	RTA	1000℃, 160sec	1000℃, 100sec
		heating rate = 4℃/sec and rapid, cooling rate = 7~20℃/sec and rapid	

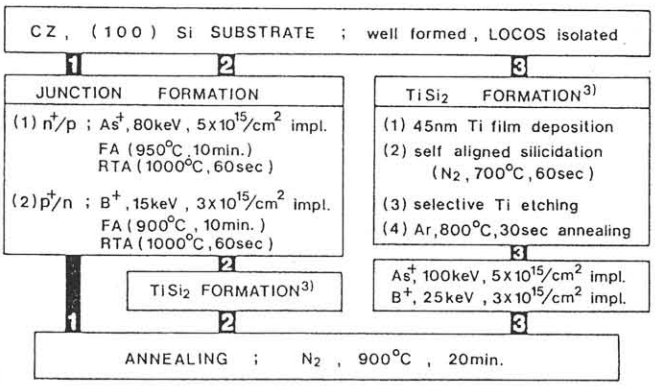

Fig. 1 Process sequences of doped layer and $TiSi_2$ formation.

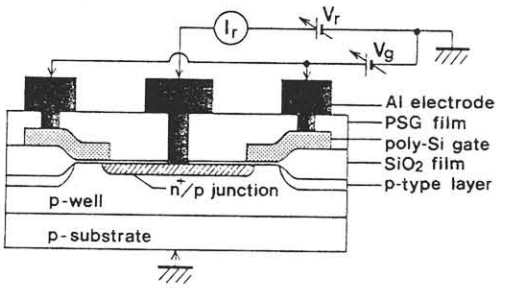

Fig. 2 Schematic cross section of gate diode.

Table 2 n^+/p junction formation conditoins and leakage current. As^+ implanted dose is $5x10^{15}/cm^2$.

		conditions and results					
		1	2	3	4	5	6
As^+ impl. energy		40 keV	40 keV	80 keV	40 keV	40 keV	40 keV
anneal. condition		950℃, 10min.	950℃, 40min.	950℃, 10min.	1000℃, 160sec	1000℃, 160sec	1000℃, 160sec
heating rate					rapid	rapid	4℃/s
cooling rate					rapid	7℃/s	rapid
junction depth		0.12μm	0.17μm	0.17μm	0.09μm	0.09μm	0.10μm
leakage	Ja(A/cm²)	3.8 E -10	2.1 E -10	2.9 E -10	3.5 E -10	4.1 E -10	4.0 E -10
Vr=5V	Jp(A/μm)	1.2 E -10	1.1 E -10	1.2 E -10	2.4 E -10	1.6 E -10	2.1 E -10

Table 3 p^+/n junction formation conditions and leakage current. B^+ implanted condition is 10keV, $2x10^{15}/cm^2$.

	conditions and results		
	1	2	3
annealing condition heating/cooling rate	900℃,15min.	1000℃,100sec rapid/rapid	1000℃,100sec 4℃/s/10℃/s
junction depth Xj	0.23μm	0.18μm	0.20μm
leakage Ja(A/cm²)	2.6 E -10	3.5 E -10	3.1 E -10
Vr=-5V Jp(A/μm)	2.2 E -10	5.1 E -10	4.5 E -10

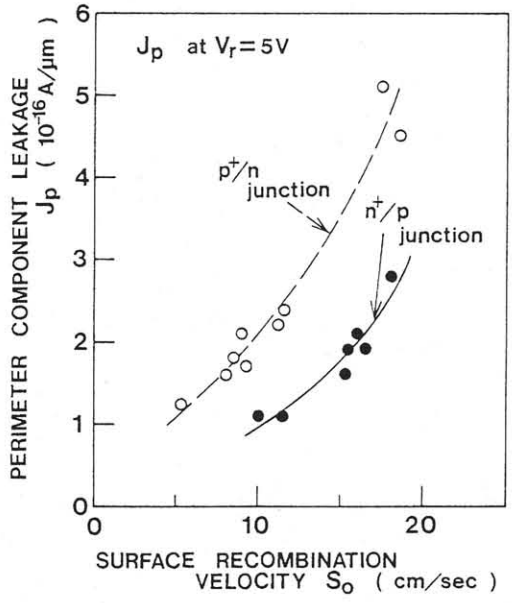

Fig. 3 Relationship between perimeter leakage and surface recombination velocity.

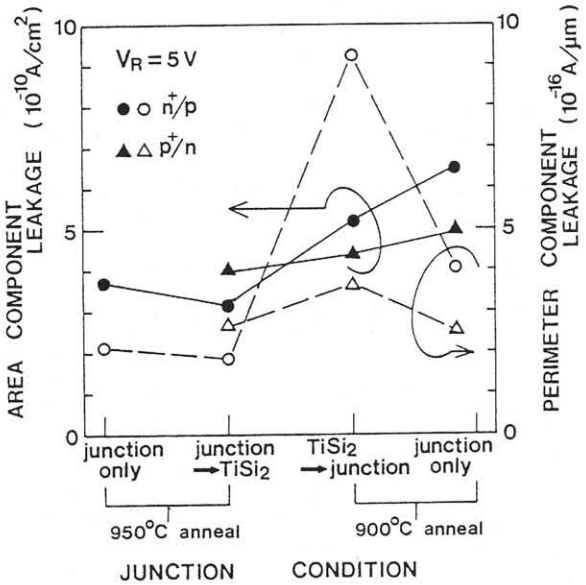

Fig. 4 Dependency of various process sequences on leakage current.

Table. 4 Characteristics of CMOS transistor fabricated by optimum conditions.

		source / drain formation conditions		
		junction only	junction → $TiSi_2$	$TiSi_2$ → junction
BVds (V) [Vg=0V]	n channel	14.7	14.5	12.4
	p channel	11.3	12.4	7.9
g_m (S) [Leff=0.5μm]	n channel	1.38×10^{-3}	1.38×10^{-3}	1.38×10^{-3}
	p channel	0.90×10^{-3}	1.05×10^{-3}	1.05×10^{-3}
ΔL (μm) [Vg=0V]	n channel	0.26	0.29	0.26
	p channel	0.29	0.31	0.23
Isub/Id [Leff=0.5μm]	n channel	3.1×10^{-3}	2.6×10^{-3}	3.1×10^{-3}
	p channel	5.0×10^{-6}	2.2×10^{-6}	$> 5\times10^{-6}$
Xj (μm)	n^+/p junction	0.16	0.18	0.16
	p^+/n junction	0.28	0.31	0.25