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Degradation of MOS Characteristics Caused by Internal Stresses in Gate Electrodes

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In WSix/poly Si-gate electrodes with tensile stresses, positive-charge trap centers accumulate at the gate-electrode/SiO2 interfaces, reducing breakdown voltages of the gate oxides. Compressive stresses in W-gate electrodes increase surface state generation and degradation rate of MOSFET transconductances caused by hot carriers at the SiO2/Si-substrate interfaces. These results show that charges accumulate at the interfaces in which compressive strains are formed in SiO2 layers by the external forces.

1. INTRODUCTION

As MOSLSI integration advances, $MoSi_2$/poly Si, WSi_2/poly Si or refractory metals are increasingly applied as low-resistance gate electrodes and interconnections. These gate electrodes replace the poly Si-gate, previously the most widely used gate. The internal stresses of these new gate electrodes are $\sim 10^9$ N/m^2, one order of magnitude greater than that of poly Si-gate. Jaccordine and Schlegel[1] state that stress of about 10^8 N/m^2 arising in the SiO_2/Si-substrate interface from the thermal expansion coefficients of SiO_2 and Si should affect charge density. Thus it can be assumed that strong internal stresses of the above new gate electrodes affect MOS device properties. This report describes cases where internal stresses in new gate electrodes seem to reduce MOS device reliability. These cases are reduced breakdown voltages of gate oxides (SiO_2) and increased MOSFET characteristic degradation caused by hot carriers. From these reults, a geometrical model is formulated explaining the relationship between MOS characteristics at interfaces and stresses in gate electrodes.

2. EXPERIMENTAL

Preparation of WSi_x/poly Si and W films

The substrates used in fabricating test samples are p-type (100) 10Ω · cm Si wafers. The tungsten films of 100~350 nm-thicknesses are formed on 10~20 nm-thick gate-oxides using a dc magnetron sputtering equipment. To fabricate WSi_x/poly Si gates, phosphorous-doped poly Si layers of 50~350 nm-thicknesses are first formed. Tungsten silicide is then deposited using a cold wall LPCVD equipment on these layers.

Measurement of film internal stresses

Silicon wafer bending caused by film internal stresses is measured to calculate these stresses. Bending value is obtained by measuring wafer curvature with an optically levered lased-beam method before and after film deposition.

Measuring MOS characteristics

The Fowler-Nordheim current injection technique proposed by Solomon[2] is used to determine charge trap centers near gate-electrode/SiO_2 interfaces. If trap centers at the interfaces have positive charge, hysteresis of I-V characteristics can be observed before and after positive-charge trap

centers are neutralized by electron injection into SiO_2 from gate-electrodes, as shown in Fig. 1. The voltage shift (ΔV_{1-2}) is proportional to trap center density.

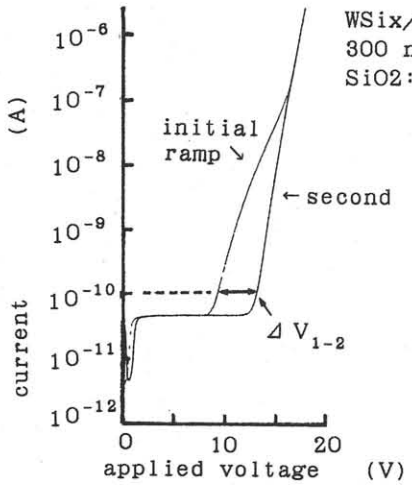

Fig. 1 Fowler-Nordheim characteristics of a WSix/poly Si-gate

Fine MOSFET surface state density (D_{it}) is measured by the charge-pumping current method described by Elliot[3].

The degradation of MOSFET transconductance (g_m) is caused by hot carrier injections into SiO_2 from Si-substrates. It is evaluated by applying the stress voltage of a gate voltage and source-drain voltage at maximum substrate current. Lifetime (τ) is defined as the time required for stress voltage application to reduce g_m 10 percent from the initial transconductance (g_{mo}).

3. RESULTS AND DISCUSSIONS

3.1 Internal stresses in W and WSi_x films

The internal stresses in W films can be controlled by Ar pressure during W deposition.[4] Stress values in films used as gate electrodes are set at highly compressive stresses of ~ 1.5 x 10^9 N/m^2. Initial compressive stresses in films change to tensile stress of ~4 x 10^8 N/m^2 after 900 ~ 1100℃ annealing as shown Fig. 2.

Internal stresses in WSi_x films decrease as silicon increases in film composition. The as-deposited WSi_x films with x = 3.0 used in this study have tensile stresses of ~ 5 x 10^8 N/m^2.

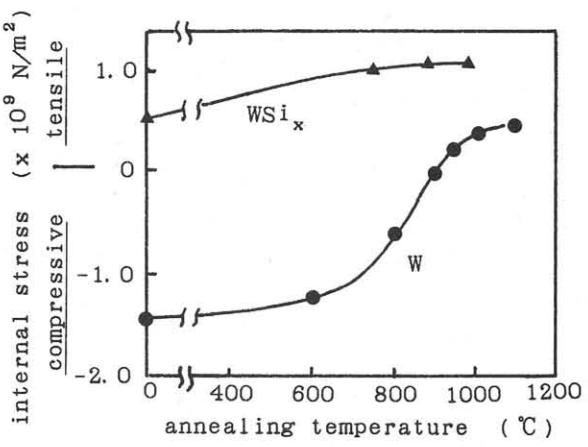

Fig. 2 Dependence of internal stresses in W and WSix films on annealing temperature

3.2 Trap centers at gate-electrode/SiO_2 interfaces

To clarify effects of forces caused by internal stresses in gate electrodes, ΔV_{1-2} (cf. Fig. 1) is measured as function of gate electrode thickness.

Gate electrodes with tensile stresses

Hysteresis is observed in I-V characteristics of leak current in SiO_2 layers on the WSi_x/poly Si-gate capacitors, as shown in Fig. 1. MOS capacitors which are not annealed before WSi_x/poly Si layers are patterned to gate electrodes exhibit the following characteristics. The dependence of ΔV_{1-2} on thickness of WSi_xlayers is examined for capacitors with 100 nm-thick poly Si layers under tungsten silicide layers, as shown in Fig. 3. It is clear that when forces generated by tensile stresses in WSi_x layers affect gate oxides, trap centers are generated at gate-electrode/SiO_2 interfaces proportional to the magnitude of these forces. The dependence of ΔV_{1-2} on poly Si layer thickness is also observed when tungsten silicide layers are of constant thickness (300 nm). The ΔV_{1-2} increases as poly Si layer thickness decreases. This indicates that poly Si layers buffer the forces applied to SiO_2 layers. Samples whose WSi_x/poly Si layers are annealed before be-

ing patterned to gate electrodes ("pre-annealing") exhibit almost no hysteresis of I-V characteristics, as shown in Fig. 3. The

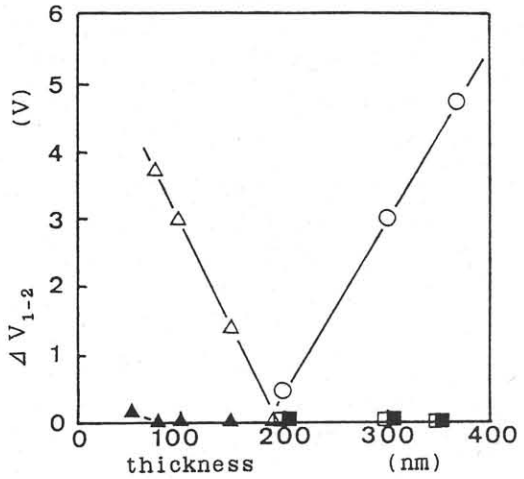

Fig. 3 Dependence of hysteresis voltages, ΔV_{1-2}, on gate-electrode layer thickness. (1)WSix/poly Si-gate: ○ WSix variable (poly Si: 100 nm) non pre-annealed; △ poly Si variable (WSix: 300 nm) non pre-annealed, ▲ pre-annealed. (2)W-gate: □ non pre-annealed; ■ pre-annealed

difference in characteristics between non pre-annealed and pre-annealed samples is caused by the difference in magnitude of the strains accumulating at gate-electrode/SiO_2 interface under the edge of gate electrodes by annealing processes after patterning. In pre-annealing samples, the change of film properties, namely grain growth, transition of structure of crystals (amorphous ⇒ hexagonal ⇒ tetragonal) and corresponding volume shrinkage is completed during annealing. As a result, pre-annealing can reduce internal strains in SiO_2 layers caused by annealing after patterning. This pre-annealing has a retardant effect on the dielectric breakdown of gate oxides. Breakdown voltages on non pre-annealed and pre-annealed samples with WSi_x/poly Si-gates are compared in Fig. 4.

Gate electrodes with compressive stresses

Stress magnitudes in the tungsten films as deposited for gate electrodes (~ 1.5 x 10^9 N/m^2, compressive) are about three times higher than those of WSi_x/poly Si-gates and the change in internal stresses caused by annealing is much greater. However, the ΔV_{1-2} of both the non pre-annealed and pre-annealed W-gate MOS capacitors is under the detectable limit as shown in Fig. 3. The hystograms of the breakdown voltages of MOS capacitors show almost no degraded elements even on the non pre-annealed samples as shown in Fig. 4.

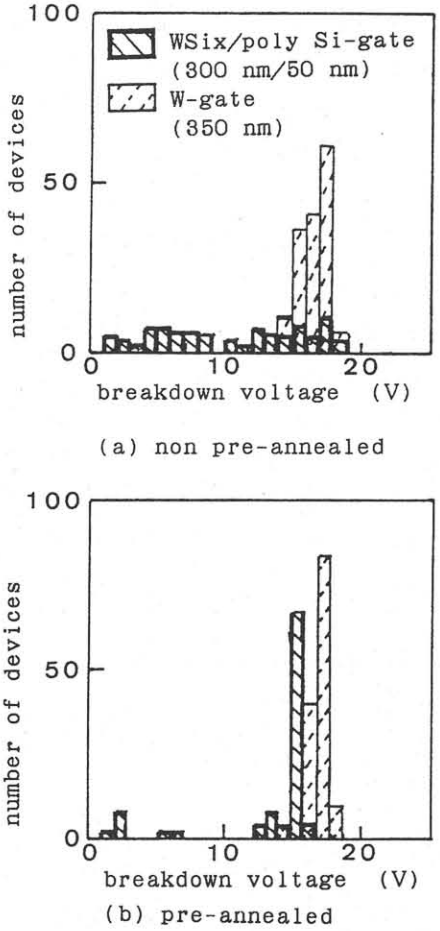

Fig. 4 Comparison of breakdown voltages for 18 nm-thick gate oxides

3.3 MOS characteristics at the SiO_2/Si-substrate interfaces

This section discusses the influence gate electrode internal stresses on the generation of surface state densities and the degradation of MOSFET transconductances caused by hot carrier injection.

Gate electrodes with compressive stresses

Author has previously investigated the influence of compressive internal stresses in W gates on transconductance degradation

caused by hot carrier injections.[5] The main points of this investigation are as follows. Compressive stresses in W-gate cause strains in silicon substrates and SiO_2 under the edges of gate electrodes. This increases the number of surface states. As a result, these internal stresses increase g_m degradation due to hot carriers. Lifetime , τ, defined in section 2, degrades as the exponential function of forces caused by internal stresses in W-gates applied to gate oxides. pre-annealing improves the W-gate device characteristics to poly Si device level.

Gate electrodes with tensile stresses

MOSFETs with LDD (Lightly Doped Drain) and WSi_x/poly Si-gate are used to investigate of g_m degradation on the application time of stress voltages. There is no observable difference in the g_m of both non pre-annealed and pre-annealed devices as shown in Fig. 5. Their degradation is almost comparable to that of poly Si gate devices.

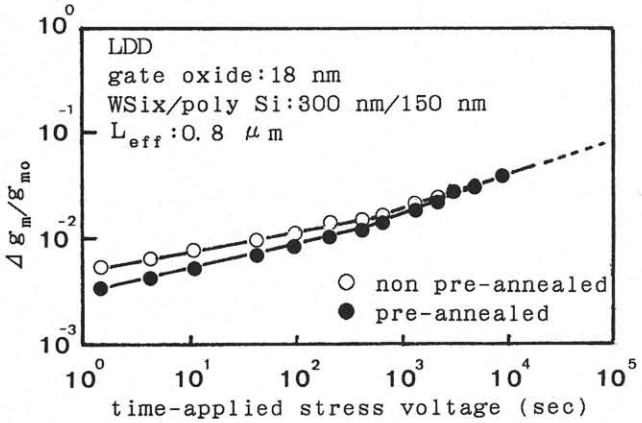

Fig. 5 Degradation of g_m of WSix/poly Si gate MOSFETs.

4. SUMMARY

It is shown that when gate-electrode internal stresses are tensile, the number of positive-charge trap centers at gate -electrode/SiO_2 interfaces under the edges of gate electrodes increases with the forces caused by them. Conversely, when internal stresses are compressive, MOS characteristics at SiO_2/Si-substrate interfaces are affected by the forces applying SiO_2 layers. These affected characteristics are, specifically, surface state generation rate, and g_m degradation rate caused by hot carrier injection. These results provide a geometrical model which simultaneously satisfies two relationships between strain and MOS characteristics at the gate electrode/SiO_2 and SiO_2/Si-substrate interfaces. It is that MOS characteristics are influenced at the interfaces in which compressive strains in SiO_2 layers are formed. This model is consistent with previous experimental results[1] regarding the relationship between compressive internal stresses in thermal SiO_2 and surface states in SiO_2/Si-substrate.

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