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Correlation between Atomic-Scale Structures and Electronic Properties at Compound Semiconductor Layered Interfaces

Hideki HASEGAWA, Hideo OHNO, Tetsuya HAGA*, Yutaka ABE*,
Heishichirou TAKAHASHI**, Takayuki SAWADA***, Li HE and Hirotatsu ISHII

Department of Electrical Engineering, Faculty of Engineering
Hokkaido University , Sapporo, 060 Japan
(*:Dept. of Nuclear Eng., ** :Dept. of Metallurgical Eng., ***:presently with Dept. of Electronic Eng., University of Electro-Communications)

Correlation between atomic-scale structures and interface state properties is investigated for compound semiconductor insulator-semidonductor (I-S) and semiconductor-semiconductor(S-S) interfaces, using cross-sectional TEM, RBS, XPS and C-V techniques. Thermal, anodic and plasma CVD I-S interfaces and homo- and hetero-epitaxial MOVPE interfaces were formed on GaAs and InP. Presence of processing-introduced disorder and its remarkably strong correlation with interface state density distributions were found, being consistent with the recently proposed disorder-induced gap state (DIGS) model. A particular space and energy distribution of the DIGS allows a complete self-consistent computer reproduction of hysteresis effects in MIS C-V curves.

1. Introduction

Advanced compound semiconductor devices require more and more crucial control of layered interfaces. This paper tries to correlate atomic-scale structures of compound semiconductor insulator-semiconductor (I-S) and semiconductor-semiconductor (S-S) interfaces with the interface state properties, using cross-sectional TEM, RBS, XPS and C-V methods. The results support the recently proposed unified disorder-induced gap state (DIGS) model[1] involving formation of bonding and anti-bonding gap states induced by distortion of local bonds. A detailed electronic model of interface allows complete self-consistent simulation of hysteresis effects in MIS C-V curves.

2. TEM, RBS, XPS and C-V Characterization

Thermal, anodic and plasma CVD I-S interfaces were prepared on Si, GaAs and InP. As S/S interfaces, GaAs/GaAs regrowth interfaces with air-exposure, slightly lattice mismatched $In_xGa_{1-x}As$/GaAs interfaces (x=0.01-0.02) and highly mismatched GaAs/InP interfaces were prepared, using a standard vertical MOVPE growth system.

Cross-sectional TEM micrographs of the interfaces taken by JEOL 2000 EX and FX, are shown in Fig.1 ,for (a) PCVD SiN/GaAs, (b)as-grown anodic oxide(AGW) /GaAs, (c)annealed anodic oxide/GaAs (300°C, 3hrs), (d) SiO_2/Si and (e)regrown GaAs/GaAs (after 24 hr air exposure), respectively. As seen in Fig.1, relatively sharp transition from to crystal to amorphous phase is indicated at the I-S interfaces. However, there exists a region at the interface where the lattice image is disordered and blurred. Its width is strongly material and processing dependent, reducing in the order of from (a) to (d) in Fig.1. In Fig.1(c), the width of the blurred region is 2-3 monolayers, and in (d), only 1-2 monolayers. On the other hand, no appreciable disorder in lattice image was observed in the S-S interface in Fig.1(e). The dark field image, however, detected a blurred linear image of the width of 10-20 Å as shown on the righthand side. The result indicates that the fundamental lattice periodicity is not appreciably perturbed on average at this interface, but that there exist short range scat-

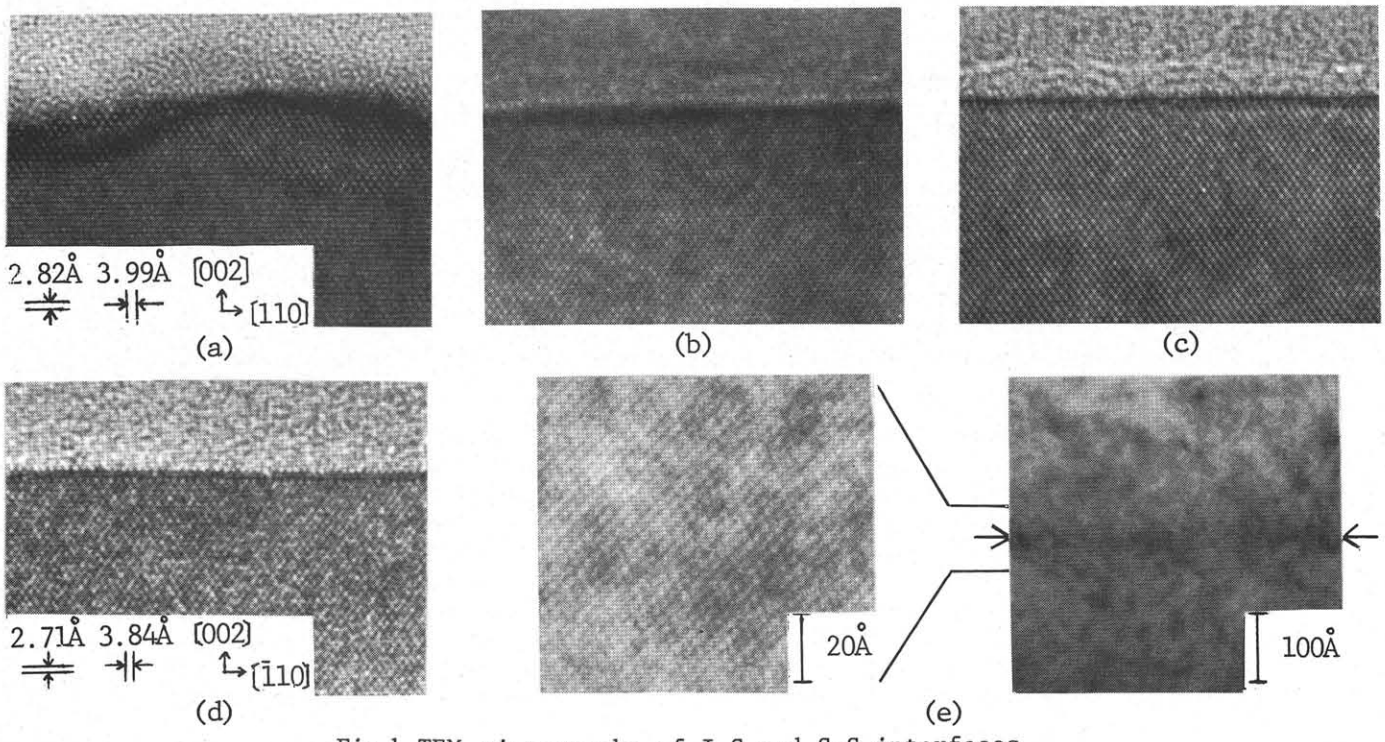

Fig.1 TEM micrographs of I-S and S-S interfaces

ters in the interface vicinity.

Electrically measured interface state density (N_{ss}) distributions of the interfaces are summarized in Fig.2. For S-S interfaces, N_{ss} was determined using Schottky C-V curves, as discussed in detail in Ref.(2). As is evident from Figs.1 and 2, a remarkably strong correlation exists between the degree of interface order and the N_{ss} distributions.

RBS study of I-S interfaces under ion channeling condition, using 1 MeV He ion probe, detected presence of surface peaks as shown in Fig.3, indicating deviation of interface atoms from their lattice sites. The surface peak height increased with the insulator thickness, showing that the deviation is processing induced.

RBS and XPS techniques were employed to determine insulator composition. An example is shown in Fig.4 for Al_2O_3/native/InP interface [3] which gave the lowest N_{ss} in the present study except for Si. Wet etching was employed for profiling to avoid composition change and differential sputtering inevitable in Ar ion bombardment. The reason for low N_{ss} was attributed to interface oxide of $In(PO_3)_x$ as confirmed by the valence band spectra reported recently.[4] As seen in Fig.4, the observed composition profile at the interface is less sharp than the transition

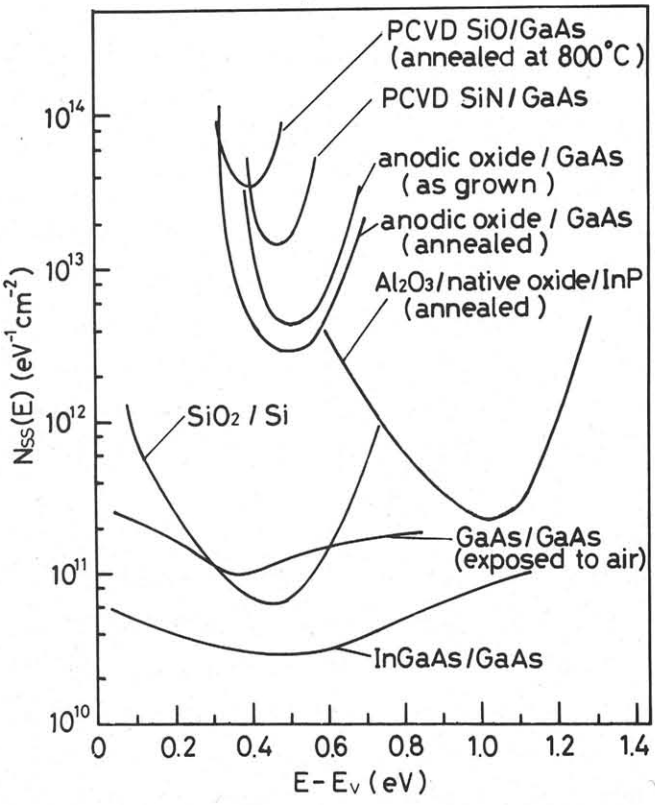

Fig.2 N_{ss} distributions of interfaces in Fig.1

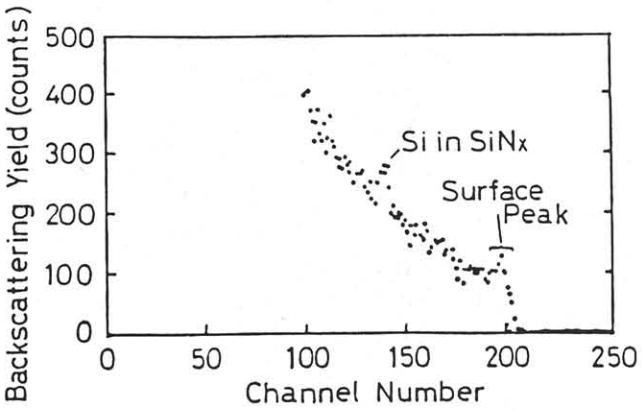

Fig.3 RBS spectrum from PCVD SiN/GaAs interface

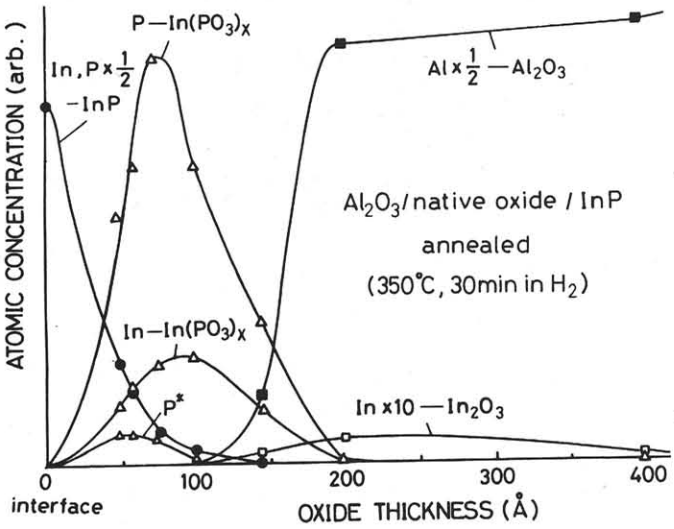

Fig.4 XPS in-depth profile of anodic Al_2O_3 /native oxide/InP I-S interface

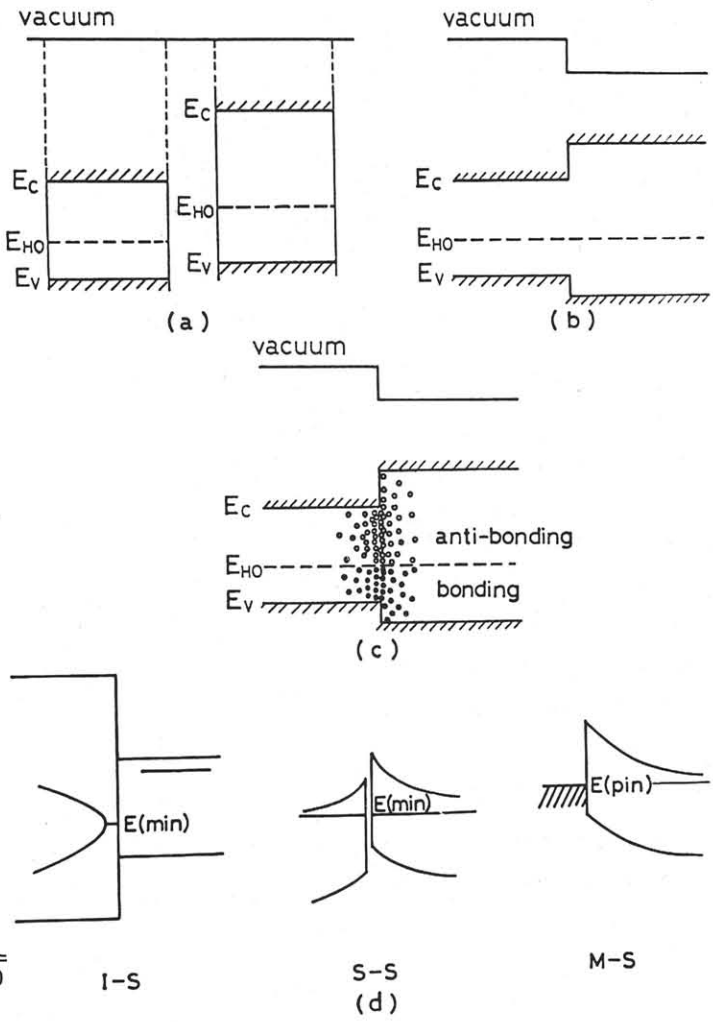

Fig.5 Electronic model of interface

from crystal to amorphous phase in Fig.1, indicating a certain amount of intermixing of host semiconductor component with insulator.

3. Electronic Model for Interface

As opposed to the usually accepted electron affinity model, we recently have proposed[5] that the band off-set of an ideal S-S interface is determined by matching the hybrid orbital energy charge neutrality level, E_{HO}, as shown in Fig.5 (a) and (b). We assume here that a similar charge neutrality level also exists in insulator and that Fig.5(b) also applies to I-S interface. As for the basic mechanism for such an alignment, we have proposed [5]that this level serves as the interface Fermi level during interface formation. This is quite different from the idea of interface dipole minimization by Tersoff[6] or originally by Flores and Tejedor.[7]

At real non-ideal interfaces, processing induced distortion of local bonds at the interface produces a DIGS continuum as shown in Fig.5(c), where bonding and anti-bonding states are distributed around E_{HO}. The model implies that larger interface disorder leads to higher N_{ss}. This is consistent with the observed presence of processing introduced disorder and its correlation with N_{ss}.

The model also implies that the energy position of the charge neutrality level, E_{HO}, is independent of processing and that the DIGS continuum restricts or even pins the interface Fermi level, E_{FI}, around E_{HO} as

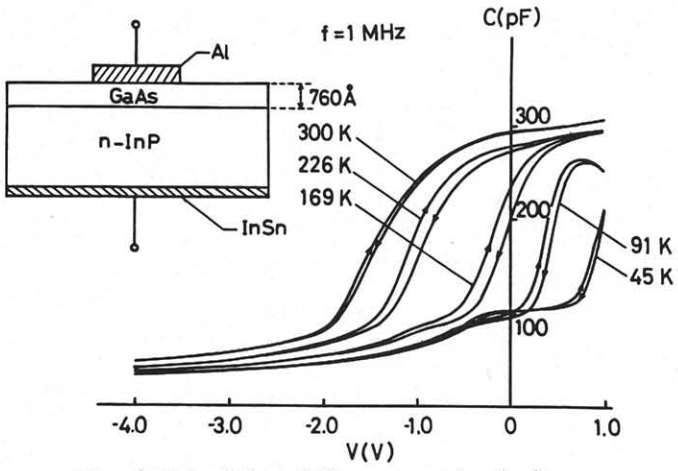

Fig.6 Schottky C-V curves including GaAs/InP interface

shown in Fig.5(d). The invariance of the energy position, E(min), for N_{ss} minimum is clearly seen in Fig.2 for GaAs I-S and S-S interfaces. Firm pinning of E_{FI} at E_{HO} at S-S interface was further directly confirmed at the highly mismatched GaAs/InP interface, as shown in Fig.6. Low temperature C-V data indicates that E_{FI} is strongly pinned, and the pinning position agrees with positions of E(min) for GaAs and InP in Fig.2. It can further be shown that the experimentally determined position of E_{HO} is in good agreement with the theoretical position based on sp^3s^* tight-binding theory.[8)]

Yet another implication of the DIGS model is the spatially distributed nature of the DIGS continuum as schematically shown in Fig.5(c). Based on such a physical picture, a self-consistent computer simulation program for capture and emission transients of DIGS continuum has been developed, and applied to the analysis of hysteresis effects in MIS C-V curves. After many trials, it was found that, by assuming a particular type of space and energy distributions shown in Fig.7(a), the experimentally observed dependences of MIS C-V curves on ramp speed and bias swing amplitude can be completely reproduced from a single set of parameters, as shown in Fig.7(b) for amplitude(V_m) dependence.

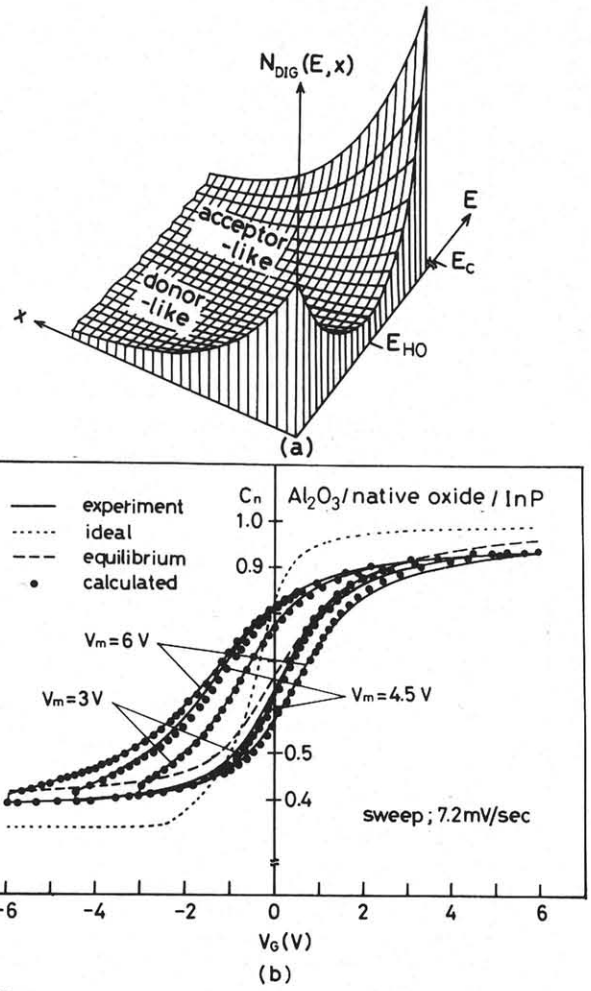

Fig.7 Experimental and simulated C-V curves

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