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Fully Symmetrical Cooled-CMOS on (110) Plane

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Advanced cooled-CMOS device technology using dual polysilicon gates, no channel implantation, (110) Si substrates, and lightly doped drains with doping concentrations of 10^{14} cm^{-2} has been developed. It was found that a p+ polysilicon gate pMOS transistor on a (110) plane is the best pMOS transistor at 77 K because of it's steeper subthreshold slope and higher hole mobility. Saturation currents and transconductances of both n and pMOS transistors have been almost equalized by the design. This fully symmetrical cooled-CMOS increases the ring oscillator speed by a factor of 1.2, and can provide flexible CMOS circuit design, making effective use of NOR gates.

INTRODUCTION

Liquid-nitrogen-cooled CMOS has received much attention as a high speed device with low power and high integration density, and the ability to overcome the MOS operational limit(1-5). A liquid-nitrogen-cooled CMOS computer system has been also developed(6). However, the device design optimized for cooled-CMOS devices has not yet been established. One problem found in the threshold control of conventional n+ polysilicon gate pMOS transistors is that the boron ions implanted in the surface freeze out, causing unusual subthreshold behavior. Therefore, the use of a p+ polysilicon gate for pMOS transistors has been proposed(7). However, carrier mobility of p+ polysilicon gate pMOS transistors is smaller than that of n+ polysilicon gate pMOS transistors because of surface channel conduction. This lowers the circuit performance and enhances asymmetry between n and pMOS drivabilities. The asymmetry results in restricted circuit design.

To solve these problems, an advanced cooled-CMOS device has been fabricated. This paper reports on a cooled-CMOS design using p+ polysilicon gate pMOS on (110) plane. This design results in remarkable pMOS improvement and fully symmetrical cooled-CMOS.

PMOS TRANSISTOR OPTIMIZATION

Threshold voltage at 77 K for conventional n+ polysilicon gate pMOS transistors can be controlled by heavily implanting boron ions im the channel. However, unusual subthreshold behavior appears in such devices, as shown in Fig. 1a(2). Therefore, another Vt control method is required. One excellent method is the use of p+ polysilicon gates(7). The work function value of p+ polysilicon is 5.25 eV and larger than that of n+ polysilicon by 1.2 eV. Therefore, low threshold values can be obtained without channel implant. Subthreshold current characteristics observed in pMOS transistors with p+ polysilicon gates are shown in Fig. 1b. Here, subthreshold swings are remarkably improved.

However, peak field-effect mobility is about 20 percent smaller than that in n+ polysilicon gate pMOS transistors as shown in Fig. 2. Hole field-effect mobilities were meausred at a source-drain field below 20 V/cm. Although measured peak mobility of n+ polysilicon gate pMOS transistors with boron channel implants of 2.5×10^{12} cm^{-2} was 640

$cm^2/V \cdot s$ at 77 K, the peak mobility of p+ polysilicon gate pMOS transistors without channel implantation was 525 $cm^2/V \cdot s$. The mobility reduction is thought to be due to stronger surface scattering, which lowers circuit performance and enhances asymmetry between n and pMOS drivabilities. To increase carrier mobility, the devices were fabricated on (110) planes. The authors recently proposed that a (110) plane is the optimum for submicrometer CMOS devices because of excellent pMOS performance(8). Based on these results, p+ polysilicon gate pMOS transistors were fabricated on (110) planes. The MOSFET current flow direction on (110) planes is in the $\langle 01\bar{1} \rangle$ direction. Measured peak field-effect mobility of p+ polysilicon gate pMOS transistors on (110) planes is 1.6 times that on (100) planes as shown in Fig. 3. This is considered to be due to lighter effective mass on (110) planes, as calculated by H. Maeda(9). Obtained results suggest that a p+ polysilicon gate pMOS transistor on a (110) plane is the best pMOS transistor at 77 K because of its steeper subthreshold slope and higher carrier mobility.

ADVANCED COOLED-CMOS DEVICE DESIGN POINTS

Based on pMOS results, advanced cooled-CMOS devices with 0.8 μm gates have been fabricated. Key design points are as follows:

(1) To obtain low threshold voltages and steeper subthreshold slopes for low temperature operation, an n+ polysilicon gate is used for an nMOS transistor and a p+ polysilicon gate for a pMOS transistor. Neither have channel implants. Both are the surface channel type. Surface impurity concentrations for n and p channel MOS transistors are 3×10^{16} and 5×10^{16} cm^{-3}, respectively.

(2) To increase pMOS mobility, the (110) plane is used for the Si substrate.

(3) Lightly doped drain structures are adopted for n and pMOS transistors. Doping concentration in the LDD region is increased to 10^{14} cm^{-2} to avoid the resistance increment caused by carrier freeze-out.

PERFORMANCE OF FULLY SYMMETRICAL COOLED-CMOS ON A (110) PLANE

In newly fabricated devices, saturation currents of pMOS transistors are about 1.6 times larger on a (110) plane than on a (100) plane at 77 K. Saturation currents of nMOS transistors are smaller by only 10 % on a (110) plane than on a (100) plane as shown in Fig. 4. Saturation currents of an n+ polysilicon gate nMOS transistor and a p+ polysilicon gate pMOS transistor on a (110) plane have been equalized. Transconductance at Vd = 5 V for a pMOS transistor is about 1.4 times larger on a (110) plane than on a (100) plane. However, transconductance of nMOS is smaller by only 6 % on a (110) plane than on a (100) plane as shown in Fig. 5. Transconductances of both transistors on a (110) plane have been also equalized. From these results it was confirmed that the cryatalline orientation dependence of p+ polysilicon gate pMOS transistors does not decrease at a submicrometer gate length. It was also indicated that the saturation current difference of n+ polysilicon gate nMOS transistors is small at a submicrometer gate length. The disappearance of the current difference could indicate that electron saturation velocity is nealy independent of the crystalline orientation.

This fully symmetrical cooled-CMOS with no channel implantation shows high saturation currents in both channel transistors, improving operational speed. Propagation delays for 0.8 μm 97-stage ring oscillators are shown in Fig. 6. Here, room-temperature optimized devices have higher well con-

centrations and threshold values are optimized to about 0.4 V at 300 K. Threshold values of liquid-nitrogen-temperature optimized devices with lower well concentrations mentioned in the former section are also optimized at 77 K. The measured delays of cooled-devices with Wp = 2Wn were 91 ps for the (100) plane and 84 ps for the (110) plane at 5 V. Here, Wn and Wp are gate widths of n and pMOS. In the (110) device with Wp = Wn, the delay was estimated to be 75 ps because of smaller gate capacitance.

Conventional CMOS circuit design generally uses NAND gates because of the asymmetry of n and pMOS drivabilities. Symmetrical cooled-CMOS could also open the door to flexible CMOS circuit design making effective use of NOR gates. Gate array designs can also be simplified.

CONCLUSION

It was found that cooled-CMOS design using p+ polysilicon gate pMOS transistors on (110) planes remarkably improves pMOS performance. Here, transistor parameters such as saturation currents and transconductances for both n and pMOS transistors have been almost equalized. This fully symmetrical cooled-CMOS increases the ring oscillator speed by a factor of 1.2, and could provide a flexible and new CMOS circuit design. This design is considered to be one solution to cooled-CMOS optimization.

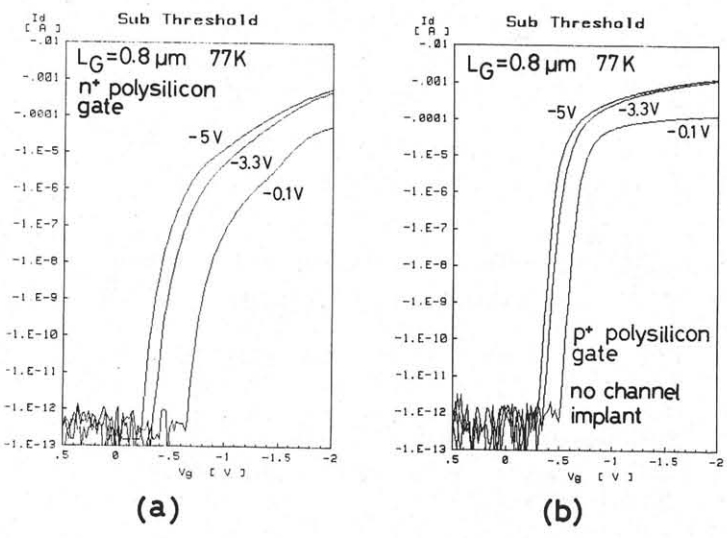

Fig. 1 Subthreshold characteristics for p+ polysilicon gate pMOS transistors.

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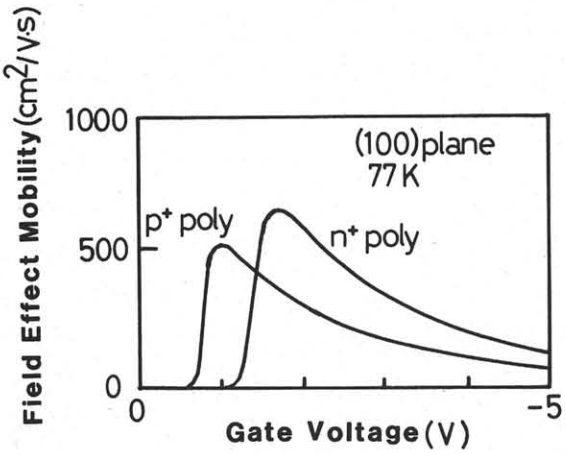

Fig. 2 Field-effect mobilities in n+ and p+ polysilicon gate pMOS transistors on a (100) plane. Gate oxide thickness is 17.5 nm and surface impurity conc. is 3.5×10^{16} cm^{-3}.

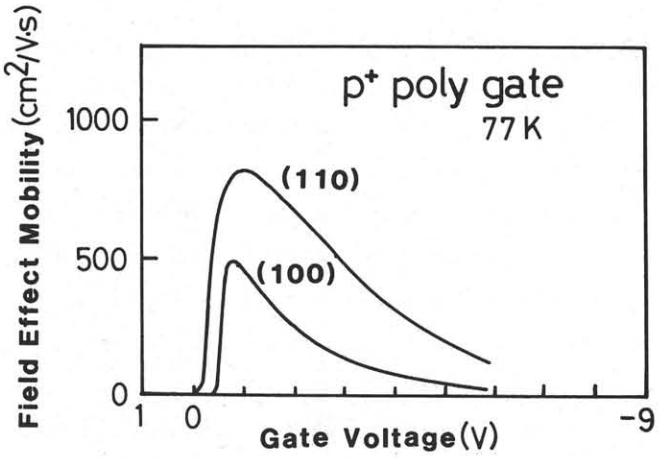

Fig. 3 Field-effect mobilities in p+ polysilicon gate pMOS transistors on (110) and (100) planes. Gate oxide thickness is 15.5 nm and surface impurity conc. is 5×10^{16} cm^{-3}.

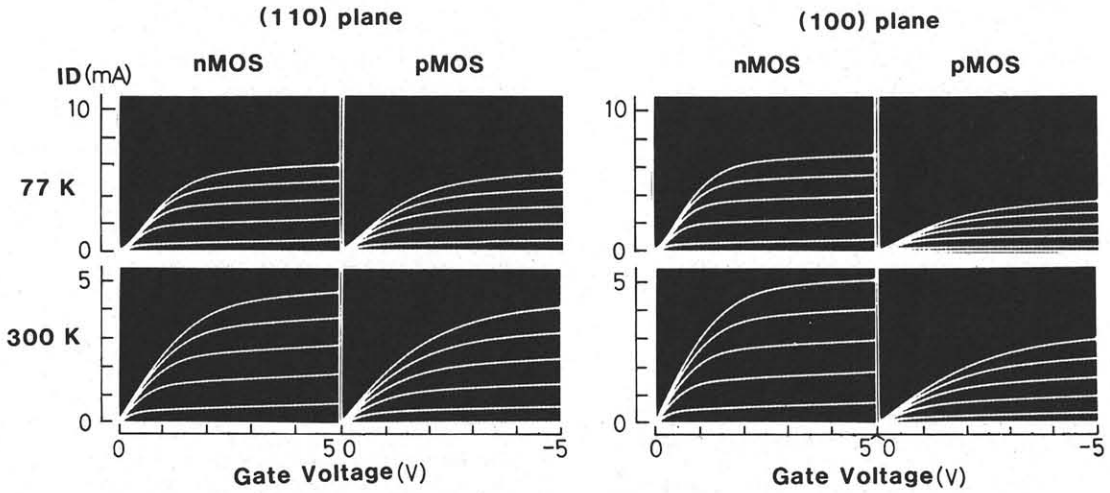

Fig. 4 Current-voltage characteristics for CMOS devices on (110) and (100) planes at 300 K and 77 K. Gate oxide thickness is 15.5 nm. Gate length and gate width are 0.7 and 10 μm for nMOS, and 0.85 and 10 μm for pMOS.

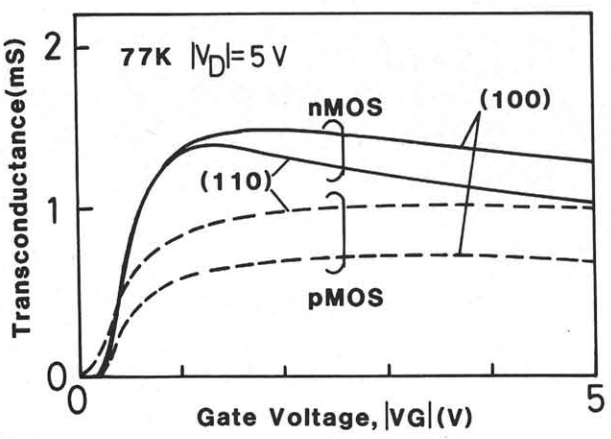

Fig. 5 Transconductances for CMOS devices on (110) and (100) planes. Gate oxide thickness is 15.5 nm. Gate length and gate width are 0.85 and 10 μm for nMOS, and 0.95 and 10 μm for pMOS.

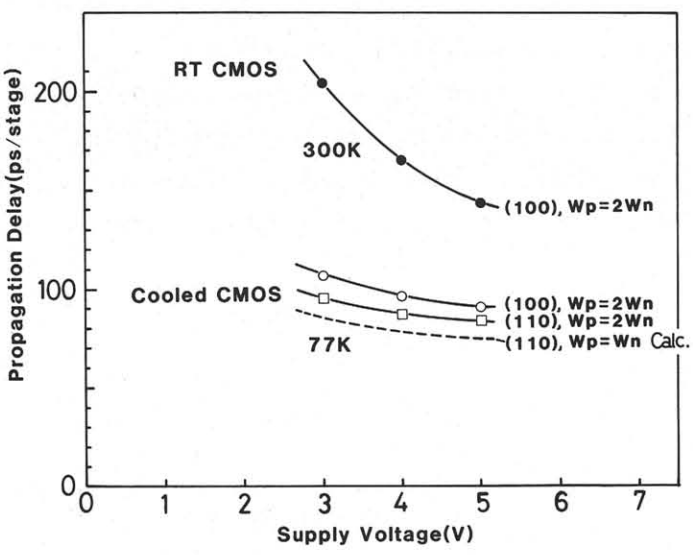

Fig. 6 Propagation delays for 0.8 um CMOS 97-stage ring oscillators.