Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 13-16

High Temperature Operated Enhancement-Type β-SiC MOSFET

Hiroo Fuma, Atsushi Miura, Hiroshi Tadano,
Susumu Sugiyama and Mitsuharu Takigawa

Toyota Central Res.& Dev. Labs.,Inc.
Nagakute-cho, Aichi-gun,Aichi-ken,480-11,Japan.

Enhancement-type β-SiC MOSFET's have been fabricated on the single crystalline β-SiC layer grown on a 3-inch Si(100) substrate by CVD. RIE technics have been applied to the MOSFET fabrication. Fabricated MOSFET's show the reasonable I-V characteristics at room temperature. The saturation tendency of the drain currents has been observed at the drain voltage above 18V, and the maximum transconductance of 200μS has been obtained in the saturated region. The MOSFET's operate even at 350°C, although the large leakage currents have been observed.

1. INTRODUCTION

For the electronic control systems in the automobile, semiconductor devices able to operate at high temperature are desired. Silicon carbide is a suitable material for this purpose because of its wide bandgap and physical stability. β-SiC single crystals have been grown on a Si or an α-SiC substrate by CVD[1,2]. Many types of devices then, have been fabricated using the β-SiC single crystals[3~6]. Recently, a depletion-mode MOSFET operation with low leakage current at 650°C was shown by Palmour et.al[7]. On the other hand, only room temperature operation of the enhancement-type MOSFET fabricated with ion implantation (I/I) has been reported[6], although an enhancement-type MOSFET is very important for the logic IC's. Source and drain formation of the MOSFET's with ion implantation is an excellent method because of the planar and self-align process. However, the annealing temperature for the recrystallization of the amorphousized β-SiC layer by I/I is very high(>1200°C)[8]. There is another method for the source and drain formation, using the reactive ion etching(RIE) which is a low temperature process and is suitable for micromachining.

In this report, enhancement-type β-SiC MOSFET's are fabricated by applying RIE technics. The β-SiC single crystalline layer was epitaxially grown on a 3-inch Si(100) substrate by CVD. I-V characteristics of the fabricated MOSFET's were measured in the temperature range from room temperature to 350°C.

2. Crystal Growth

A horizontal-type normal pressure CVD apparatus was used for the crystal growth. The 3-inch Si(100) substrate about 10' off toward the <011> direction was used to obtain the single crystalline β-SiC layer free from antiphase disorder. The Si substrate was set on a silicon carbide coated graphite suceptor which was heated by rf-induction.

At the first of the growth process, the Si substrate was etched using a $HCl-H_2$ gas system at 1100°C for 5 min. The flow rates of HCl and H_2 gases were 100cc/min and 12ℓ/min, respectively. And, following the initial carbonization process, epitaxial growth process was carried out at about

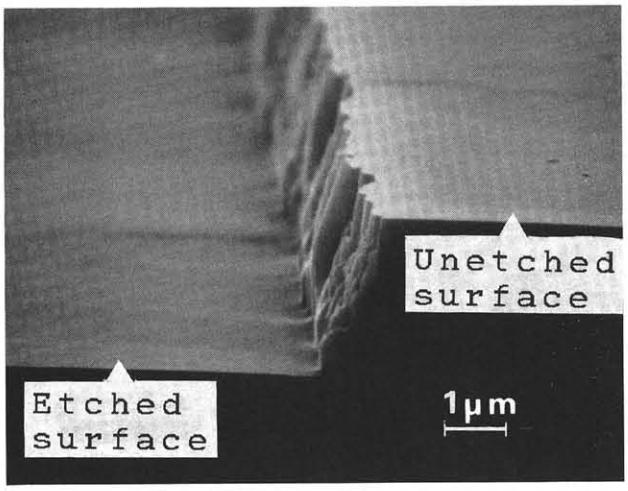


Fig.1 SEM micrograph of the β-SiC layer after RIE.

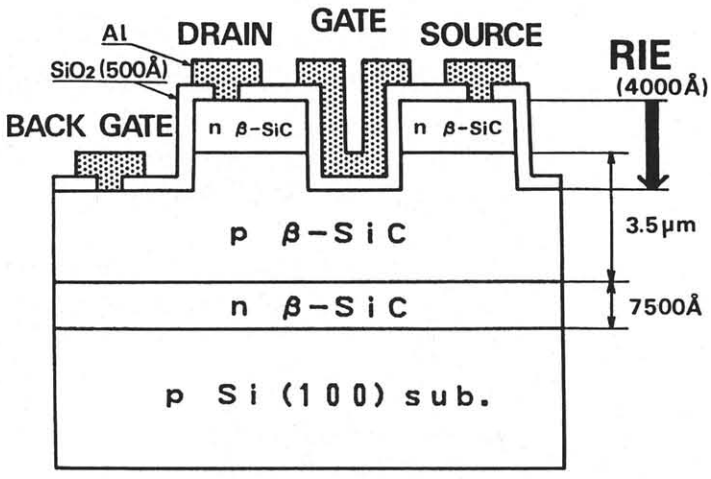


Fig.2 Schematic cross sectional structure of a β-SiC MOSFET.

1320°C using a C_3H_8-SiH_4-H_2 gas system. Gas flow rates were as follows, (H_2) ; 12ℓ/min constant during each processes, (C_3H_8) ; 6cc/min at carbonization and 3cc/min at epitaxial growth, and (SiH_4) ; 5cc/min at epitaxial growth. Growth of a p-type β-SiC layer was carried out by adding the B_2H_6 gas of 0.05cc/min.

Growth rate was about 1.5μm/hr at the center region of the 3-inch Si substrate. The β-SiC layer grown for 3hr without the addition of B_2H_6 gas showed the n-type conductivity and the carrier concentration of $6\times10^{16}cm^{-3}$ - $1.5\times10^{17}cm^{-3}$.

3. RIE of β-SiC

Reactive ion etching of the β-SiC layer was carried out using the CF_4 + 17% O_2 mixture gas with a parallel-plate-type RIE apparatus. The etch rate of the β-SiC layer was about 500Å/min at the rf-power of 0.24 W/cm^2 and at the pressure of 3.8 Pa. The surface of the etched β-SiC layer is shown in Fig.1. Very smooth surface has been obtained after the etching.

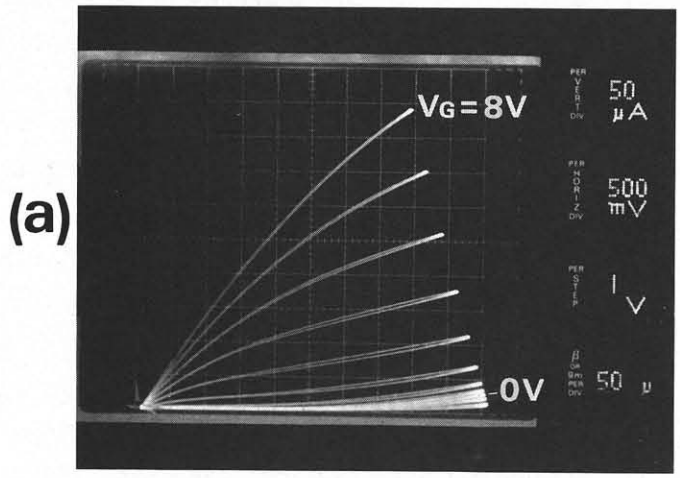
4. Device Fabrication

A schematic cross sectional structure of the fabricated MOSFET is shown in Fig.2. Fabrication process was as follows. First, the n,p and n-type β-SiC layers were grown on the 3-inch Si substrate. The n-type β-SiC layers were obtained without any additional doping gas. The lower n-type layer in Fig.2 was grown for 30min and the upper was grown for 15min. The p-type β-SiC layer was obtained with B_2H_6 doping gas, and was grown for 135min. About 3cm × 1cm size β-SiC layers with Si substrate were cleaved out for the MOSFET fabrication.

Next, β-SiC layer of 4000Å thickness was etched off except the source and drain regions by RIE. The gate insulator was formed on the β-SiC layer by the thermal oxidization in wet O_2 at 1100°C for 2 hrs. This oxidization treatment formed the oxide of about 500Å thickness on the n-type β-SiC layer. After contact holes were opened in the oxide layer, aluminum electrodes were formed. Finally, the devices were annealed in N_2 ambience at 450°C for 20min. The size of the β-SiC MOSFET is about 0.5mm × 0.6mm. And the gate length (L) and the width (W) are 20μm and 600μm, respectively.

5. MOSFET Characteristics

Fabricated devices showed the transistor operation at room temperature. Typical I-V characteristics of the MOSFET at room temperature are shown in Fig.3. At the drain voltage (V_D) lower than 3V, drain currents (I_D)



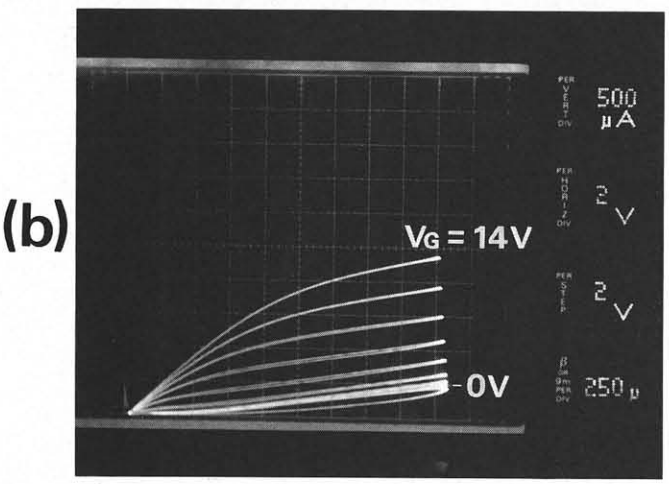


Fig.3 I_D-V_D characteristics of a MOSFET. (a) Drain voltage;0~5V, (b) Drain voltage;0~19V.

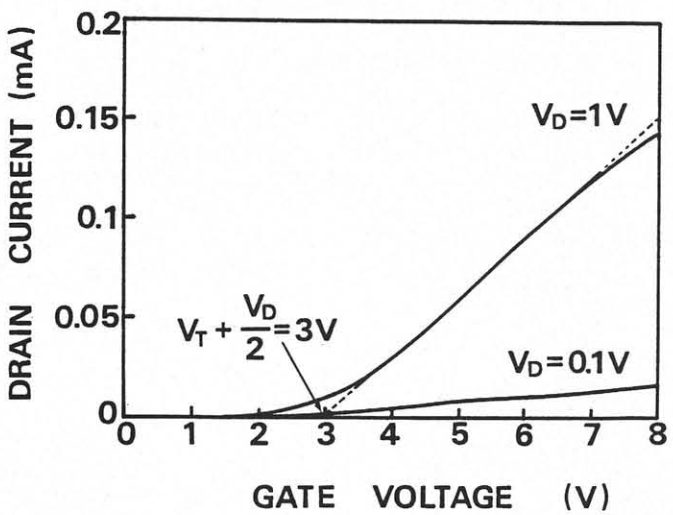


Fig.4 I_D-V_G characteristics of the MOSFET.

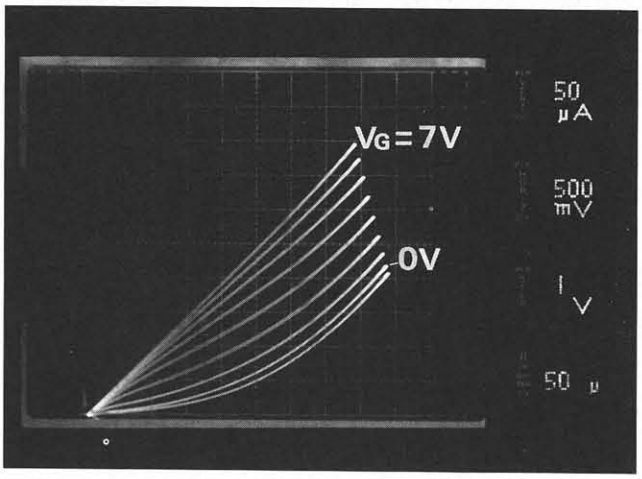


Fig.5 I_D-V_D characteristics of a MOSFET at 350°C.

flow only when the gate voltage (V_G) is above 2V. This means that the MOSFET is enhancement-type. On the other hand, drain currents flow even if the gate voltage is below 2V when the drain voltage is higher than 3V. These drain currents are supposed to be the leakage currents caused by the defects in the β-SiC crystal. The saturation tendency of the drain currents is observed at the drain voltage above 18V(Fig.3-b) and the maximum transconductance of 200μS at room temperature is obtained in the saturated region. I_D-V_G characteristics in the unsaturated region of this device are shown in Fig.4. I_D-V_G curves show linear characteristics and the threshold voltage (V_T) is about 2.5V. Transistor operation was observed in the temperature range from room temperature to 350°C, although the leakage currents increased at above 200°C. I-V characteristics of other device at 350°C are shown in Fig.5. At 350°C, large leakage currents flow at the drain voltage above 1V(Fig.5).

6. Discussion

The electron mobility(μ_e) in the inversion layer in the unsaturated region is estimated to be 15cm^2/V·sec from I_D-V_G curves (Fig.4), using a simple equation (1).

$$I_D = \mu_e \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{Tox} \cdot V_D \cdot (V_G - V_T - \frac{V_D}{2}) \quad \cdots\cdots(1)$$

where ε_{ox} is the permittivity of the oxide, and the gate oxide thickness (Tox) is supposed to be 500Å. Also, the electron mobility at the saturated region (V_D=18V, V_G=14V) is estimated to be 15cm^2/V·sec using the equation (2).

$$I_D = \frac{1}{2} \cdot \mu_e \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{Tox} (V_G - V_T)^2 \quad \cdots\cdots(2)$$

In the calculation, the drain current at V_G=0V is subtracted from the measured drain current, because the drain current at V_G=0V is considered to be a leakage current. The estimated mobilities are equal both in the unsaturated region and in the saturated region. This means that the MOSFET shows the reasonable I-V characteristics. The estimated electron mobilities are considered fairly lower compared to that in the nondoped β-SiC layer(~300cm^2/V·sec), even if the interface scattering between the oxide and the β-SiC is considered. For the reasons, following factors are supposed;(1) The deterioration of the crystallinity in the β-SiC layer by the B_2H_6 gas addition,(2) high impurity concentration in the channel region by boron doping, and (3) the roughness at the interface between the oxide and the β-SiC layer. Therefore, the electron mobility in the inversion layer is expected to be improved by further studies.

The path of the leakage currents has not been determined. But the main path is considered to be the path between a drain and a substrate[9], because at room temperature the drain current at V_G=0V is nearly equal to the leakage current between the drain and a substrate. The leakage currents are considered to be caused by the high density crystal defects[10] originated from the lattice mismatch between the β-SiC epitaxial layer and the Si substrate. The leakage currents will be reduced by the use of the high quality β-SiC crystal.

7. Conclusion

Enhancement-type MOSFET's have been fabricated on the single crystalline β-SiC layer grown on a 3-inch Si (100) substrate. RIE technics was applied to the MOSFET fabrication for the first time. Fabricated MOSFET's showed the reasonable I-V characteristics at room temperature. The MOSFET's also showed the transistor opereation even at 350°C, although the leakage currents increased.

References

1) S.Nishino, J.A.Powell, and H.A.Will ; Appl. Phys. Lett. 42(5) (1983) 460.
2) H.S.Kong, J.T.Glass, and R.F.Davis ; Appl. Phys. Lett. 49(17) (1986) 1074.
3) K.Furukawa, A.Uemoto, M.Shigeta, A.Suzuki, and S.Nakajima ; Appl. Phys. Lett. 48(22) (1986) 1536.
4) Y.Kondo, T.Takahashi, K.Ishii, Y.Hayashi, E.Sakuma, S.Misawa, H.Daimon, M.Yamanaka, and S.Yoshida ; Jpn. J. Appl. Phys. 26(2) (1987) 310.
5) H.S.Kong, J.W.Palmour, J.T.Glass, and R.F.Davis ; Appl. Phys. Lett 51(6) (1987) 442.
6) K.Shibahara, T.Saito, S.Nishino, and H.Matsunami ; IEEE Electron Device Lett. EDL-7(12) (1986) 692.
7) J.W.Palmour, H.S.Kong, and R.F.Davis ; Appl. Phys. Lett. 51(24) (1987) 2028.
8) O.J.Marsh ; Silicon Carbide 1973, 471.
9) A.Suzuki, A.Uemoto, M.Shigeta, K.Furukawa, and S.Nakajima ; Extended Abstracts of SSDM Tokyo. (1986)
10) S.R.Nutt, D.J.Smith, H.J.Kim, and R.F.Davis ; Appl. Phys. Lett. 50(4) (1987) 203.