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A New Device Structure Utilizing Atomic Layer Doping (ALD) Technology in Si Systems

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A new device structure utilizing an Atomic Layer Doping (ALD) technology in Si systems is presented. The ALD technology enables fine-structure fabrication. The new device features a lightly doped substrate with n- and p-type ALD regions. Carriers are confined in the conducting ALD region. Opposite polarity ALD regions against the conducting channel acts as punch-through stopper and, consequently, punch-through is efficiently suppressed in spite of the lightly doped substrate structure. Superior features of ALD-FETs were experimentally and theoretically demonstrated.

1. INTRODUCTION

Much effort has been devoted to miniaturize device structures and, consequently, to develop high speed and high packing density LSIs. Molecular beam epitaxial (MBE) technologies will be a breakthrough to fabricate ultra-small dimension devices.

From the viewpoint of device physics, punch-through is a major obstacle which prevents the development of ultra-short channel devices. For example, the threshold voltage steeply shifts with a decrease in the channel length. In order to suppress punch-through, a substrate should be heavily doped[1]. However, an increase in the doping level causes an increase in capacitances and deteriorates speed performances.

This paper presents a new device technology, i.e., an Atomic Layer Doping (ALD) technique and its application to device design. The present new idea is qualitatively and quantitatively evaluated utilizing computer simulation and ALD-MOSFETs are fabricated utilizing the new Si MBE technologies. Superior features of the present device are theoretically and experimentally demonstrated.

2. DESIGN CONCEPT

Miniaturization of device structures has been fundamentally guided by the shrinking theory[1]. However, as mentioned in the previous section, capacitances increase with an increase in the substrate doping level. Another obstacle inhibiting the miniaturization in the submicron range is a fluctuation of the doped impurities[2]. When the channel length is in the order of 0.1 micron range, the source-drain distance is in the same order of the interval between impurities, and the device operation is affected by the fluctuation of doped impurities. For example, the threshold voltage changes with such fluctuation[2].

In order to overcome such problems, the ALD will be a key technology. Device structures with ALD regions are schematically illustrated in Fig.1. This structure features a lightly doped substrate with heavily doped ALD regions. An ALD region is designed as a conducting channel. An opposite polarity type ALD region against the conducting channel is designed as a punch-through stopper. Due to the lightly doped substrate, the increase in

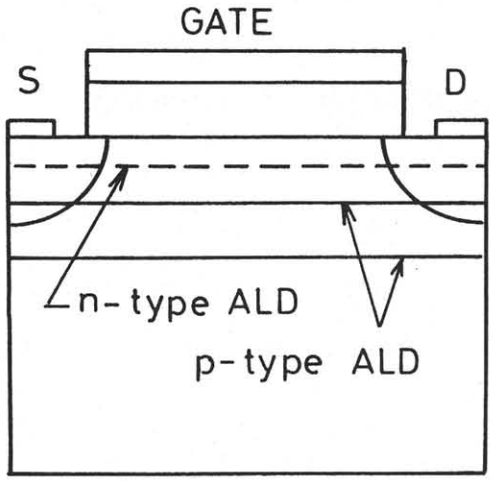

Fig. 1. Cross-sectional view of ALD-MOSFET

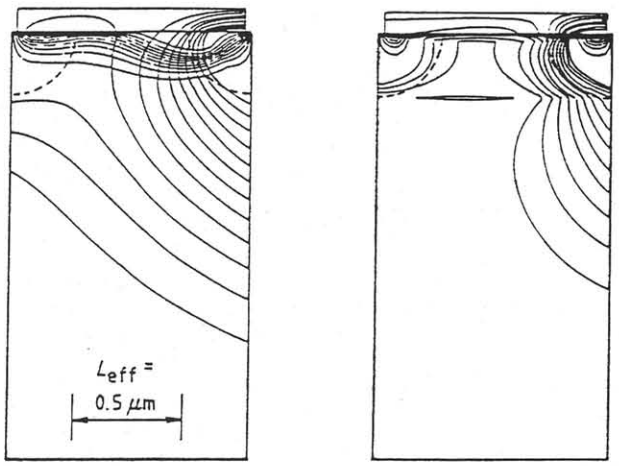

Fig. 2. Potential and current flux distribution analyzed by two-dimensional computer simulation

capacitances is suppressed and, due to the heavily doping in the ALD region, the device operation is insensitive with regard to the fluctuation.

The delta-FET[3] previously reported GaAs systems is a structure without the punch-through stopper. The opposite polarity punch-through stopper plays an essential role in a submicron range.

The operation mechanism of the proposed device is analyzed by computer simulation. Potential and current-stream lines are shown in Fig. 2. Current stream lines in the ALD device are confined in the conducting channel while they in the conventional MOSFET are widened in the depth direction.

Potential contours in the ALD devices. are pinned along the ALD region designed as punch-through stoppers. By pinning the potential contours, the drain depletion region cannot expand toward the source. That is, punch-through is suppressed. It is said that the opposite polarity type ALD region effectively suppresses punch-through.

In the present analysis, two p-type layers are formed in the Si substrate. One is situated near the n-type channel. The other is at the deep portion. The shallow (former) layer suppresses the expansion of the current flux in the depth direction. The deep one also suppresses the expansion of the potential contours toward the source direction. In order to efficiently suppress punch-through, the deep one should be situated at the position where the expansion of the potential contours becomes the maximum. In the present analysis, the depletion layer is designed at the 300 nm depth.

3. ALD TECHNOLOGY

A new process technology is developed for fabricating n- and p-type ALD regions in Si. Sb and Ga atoms are used for forming the n-type channel and p-type punch-through stopper regions, respectively.

An Sb ALD-region fabrication process sequence is illustrated in Fig. 3. Sb atoms were accumulated from the effusion cell at the substrate temperature around 650°C to grow a doped one monolayer (the top view in Fig. 3). These atoms are thermally stable on Si(100) around this temperature.

The Sb surface concentration is controlled by thermal desorption. When the substrate temperature was raised up to 750 C, excess Sb atoms were sublimated. Experimentally, the

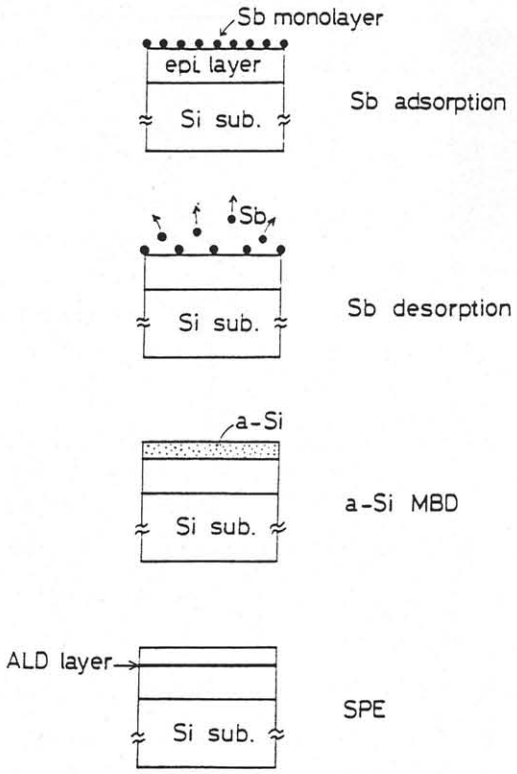

Fig. 3. Process sequence of ALD fabrication

logarithmic Sb concentration was inversely proportional to heating time. When the concentration and heating time are defined as N and t, N is given by

$$N \quad \exp(-t/\tau).$$

Here, τ is a constant. Its value is, for example, 110 seconds at the substrate temperature of 750°C.

After the control of the surface concentration, amorphous Si was grown on the substrate at the room temperature and recrystallized using solid phase epitaxy (SPE) to suppress the surface segrigation of doped atoms. The Sb diffusion coefficient in a-Si is very small. Consequently, a buried ALD region having a delta-function like doping profile is formed in Si crystal.

A p-type ALD region in Si is formed by the same process sequence using Ga atoms. As an application of the ALD technology, an ALD-MOSFET with n- and p-type buried layers is fabricated and electrical characteristics are demonstrated in the following section.

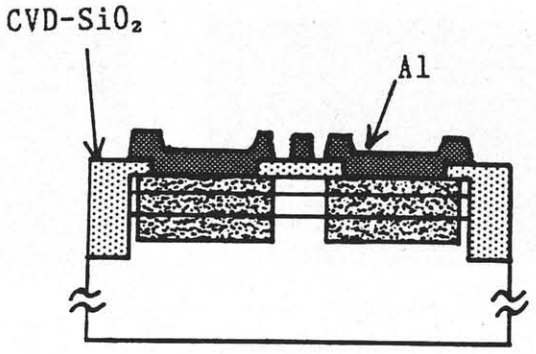

Fig. 4. Cross-sectional view of fabricated ALD-MOSFET

4. ALD-MOSFET FABRICATION

ALD-MOSFETs were fabricated on p-type 1000 ohm-cm Si(100) wafers. A cross-sectional view of the ALD-MOSFET is shown in Fig. 4. The n- and p-type ALD regions were buried at 30 nm and 300 nm depths, respectively. The latter acts as a punch-through stopper.

P^+ ions were implanted at 30 keV with 1×10^{15} cm^{-2} to form the source and drain regions. Low temperature annealing ($\sim 600°C$) was carried out to prevent the diffusion of doped atoms. The gate oxide consisted of 60 nm-thick CVD-SiO_2 deposited at 400°C. Device isolation is performed by a mesa-structure. Conventional structure MOSFETs were also fabricated under the same process condition except for the ALD fabrication process.

5. ELECTRICAL CHARACTERISTICS

Measured current-voltage characteristics of the ALD and conventional MOSFETs with the channel length of 2 μm are shown in Fig. 5. Drain currents in the ALD-FET are completely pinched-off under the reverse gate-bias conditions. However, drain currents in the conventional MOSFET cannot be pinched-off even though the high reverse bias voltage is supplied at the gate electrode. This is due to punch-through. Thus, it can be said that the ALD structure has a superior feature for suppressing punch-through.

Electrical properties of ALD-FETs in a short channel range is quantitatively evalu-

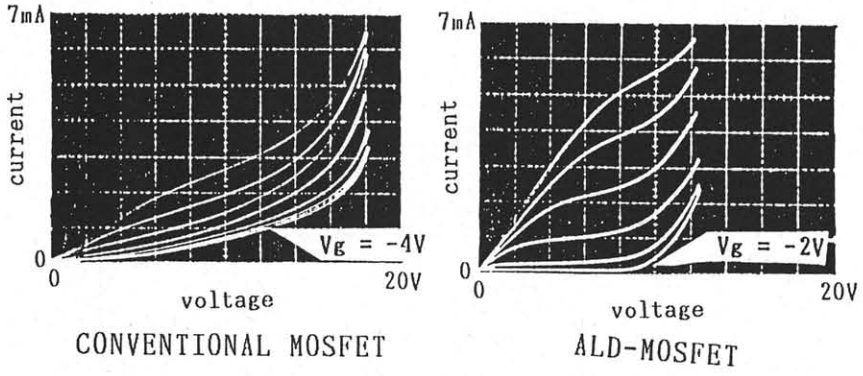

Fig. 5. Current-voltage charascteristics of ALD and conventional MOSFETs

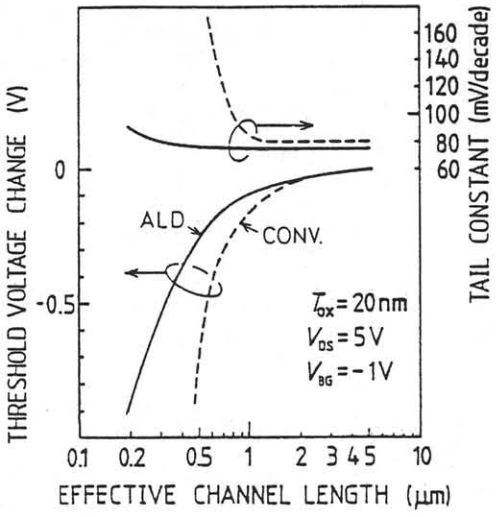

Fig. 6. Threshold voltage analysis with regard to channel length

ated using computer simulation. The threshold voltage of the ALD-FET can remain to be a constant even in a half-micron range, as shown in Fi. 6.

For reference, a conventional structure MOSFET is analyzed. Here, a doped substrate is used for suppressing punch-through. Nevertheless, the steep change in the threshold voltage appears in the range of 0.5 - 1 μm. When the minimum channel length below which the threshold voltage is steeply droped is compared between the ALD and conventional MOSFETs, the minimum length for the ALD-FET is shorter about 0.2 - 0.3 μm than that for the conventional FET. Further, the tail constant in the subthreshold region of the ALD-FET can keep a constant even in a quarter micron range. ALD-FETs can show excellent features in a very short channel region.

From the viewpoint of capacitance components, as discussed in Sec. 2, capacitance values are small due to a lightly doped substrate structure. Thus, it is concluded that the ALD structure can provide a very short channel device without an increase in capacitances and will perform a high speed operation.

6. SUMMARY

An Atomic Layer Doping (ALD) technology in Si systems has been reported. As an application, ALD-MOSFET were fabricated. Measured current-voltage characteristics showed that punch-through is efficiently suppressed. Electrical properties in a submicron channel length range is evaluated using computer simulation. It is clarified that the threshold voltage shifts in a 1/4 - 1/2 micron range. Superiority features of the ALD device were experimetally and theoretically demonstrated. The ALD structure is a candidate for ultra-short channel device development required of the next stage LSIs.

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