Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 21-24

A Complete Self-aligned-gate LID-MOS Technology

Hiroshi Inokawa and Toshio Kobayashi

NTT LSI Laboratories
3-1, Morinosato Wakamiya, Atsugi-shi,
Kanagawa Pref., 243-01 Japan

An advanced lifted-diffused-layer MOS (LID-MOS) technology was developed for future scaled devices. In this technology, relative positions of gate, polysilicon source/drain diffused layer and field insulator are exactly determined by a self-alignment method. The fabricated n-channel MOSFETs exhibit a high transconductance of 173 mS/mm and a low drain leakage current of $\sim$0.1 pA/μm at V_D = 3 V. The feasibility of the new LID-MOSFETs was successfully demonstrated by incorporating them in a 1/256 frequency divider.

1. Introduction

As the size of MOSFETs is reduced, it becomes increasingly important to reduce the source/drain parasitic capacitance and resistance. Toward this end, self-aligned structures such as LID-MOS[1], SST-CMOS[2], SAPSD-LDD[3] and UPMOS[4] have been proposed. In these structures, source/drain diffused layers are elevated on a thick field insulator using polysilicon extensions to within a short distance of the gate. For all of the structures mentioned above, however, the relative positions of gate, polysilicon diffused layer, and field insulator are not determined entirely by self-alignment, and the extent they can be scaled is limited. In this report, a new self-aligned LID-MOS technology is introduced, in which the relative positions of these three components are exactly determined, and the feasibility of the new LID-MOS technology for LSIs is demonstrated. A new planar-type LID-MOS structure is also proposed, which does not require epitaxial growth and is better suited than the conventional LID-MOS structure for further scaling.

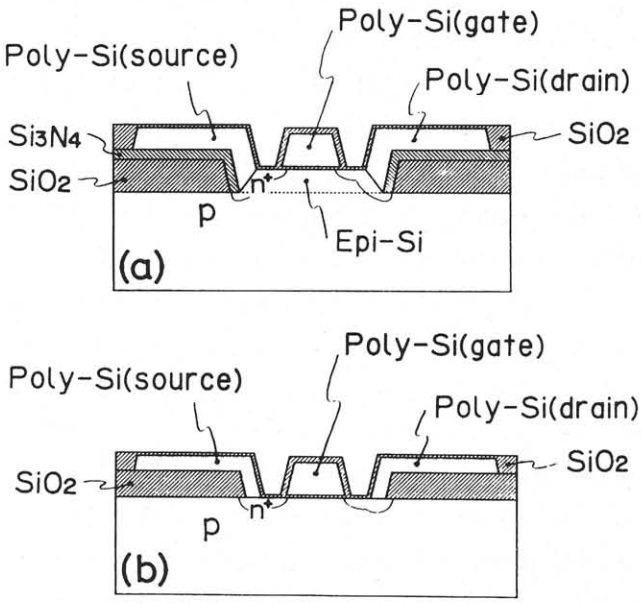


Fig. 1 Cross-section of LID-MOSFETs. (a) Mesa-type LID-MOSFET. (b) Planar-type LID-MOSFET.

2. Structure and fabrication process

Figure 1 shows the new LID-MOS structures. Figure 1 (a) is a mesa-type structure in which the active region exists in an epitaxial silicon mesa, and Fig. 1 (b)

is a planar-type structure in which the active region exists in substrate silicon. Initial fabrication steps of the mesa-type structure are (1) formation and patterning of a field insulator and (2) simultaneous deposition of epitaxial silicon on the exposed area and polysilicon over the insulator. Fabrication steps of the planar-type structure are (1) field oxidation and the 1st polysilicon deposition, (2) etching of the 1st polysilicon and the oxide to expose a channel region, and (3) deposition and anisotropic etching of the 2nd polysilicon to form polysilicon sidewalls. In both structures, n-MOS was fabricated with p-type substrate, and the epi- or poly-silicon was not intentionally doped.

After these steps, both structures undergo the same fabrication steps--LOCOS isolation, gate oxidation and gate polysilicon deposition. Then the gate polysilicon is patterned by the self-alignment method shown in Fig. 2. In this method, first, a planarization resist is coated on the wafer (Fig. 2 (a)). Second, the resist is etched back exposing the top surface of the gate polysilicon (Fig. 2 (b)). Finally, the gate polysilicon is etched using the remaining resist as a mask (Fig. 2 (c)). Figure 3 shows a cross-sectional SEM view of the fabricated structure. By the use of the self-alignment method, a gate is placed exactly in the middle of the groove between the polysilicon diffused layers.

This is followed by a source/drain implantation using the gate as a mask. In some wafers, a dopant was further added only to the polysilicon to reduce the series resistance and the drain leakage.

3. Device characteristics

Table 1 summarizes the examined wafers. The samples are varied as to device structure and the presence or absence of

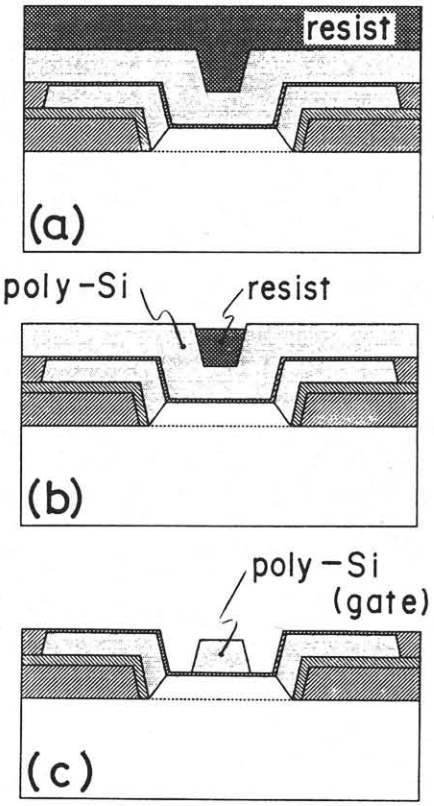


Fig. 2 Fabrication steps for the self-aligned gate. (a) Resist coating. (b) Resist etching. (c) Gate polysilicon etching.

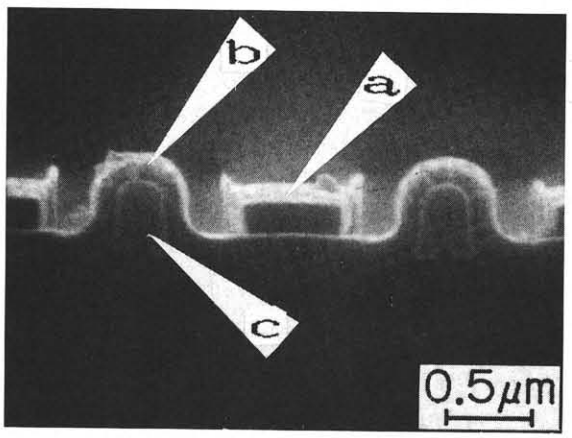


Fig. 3 Cross-sectional view of the LID-MOSFET consisting of the self-aligned (a) gate, (b) polysilicon diffused layer, and (c) field insulator.

Table 1 List of investigated wafers.

SAMPLE No.	STRUCTURE	POLY DOPE
# 1	PLANAR	NO
# 2	MESA	NO
# 3	MESA	YES

additional polysilicon doping. Gate oxide thickness is fixed at 10 nm. All of the fabricated LID-MOSFETs, with gate lengths ranging from submicron to 50 μm, exhibited normal FET characteristics. This indicates that the fabrication process of the self-aligned gate is stable and scarcely affected by the gate size. Differences between the wafers exist mainly in the parasitic series resistance and in the drain leakage current.

Figure 4 shows the subthreshold characteristics of FETs with a 10-μm gate length and a 50-μm gate width, measured at V_D = 3 V. Drain leakage current of nearly 1 nA in #1 and #2 is reduced to a few pA in #3. This is presumably because the additional doping to the source/drain polysilicon drives the junction away from the polysilicon region. Subthreshold slopes are 81 mV/decade for all three.

Figure 5 shows the dependence of the transconductance, G_m, on effective channel length, L_{eff}, at V_D = 3 V. #3 has large G_m values for all gate lengths. The maximum G_m's for #1, #2 and #3 are 86, 71 and 173 mS/mm, respectively. These differences are caused by the differences in the parasitic series resistance. The sheet resistance of the polysilicon diffused layer and the source/drain series resistance (R_S + R_D) are 370 Ω and 4.6 kΩ μm for #1, 710 Ω and 7.4 kΩ μm for #2, and 55 Ω and 540 Ω μm for #3. The smaller resistance for #3 is the result of the additional doping. The difference in the resistance between #1 and #2 originates from the difference in crystalline quality of the polysilicon.

From the results described above, it can be concluded that the new self-aligned LID-MOS with additional polysilicon doping exhibits several remarkable characteristics such as low parasitic resistance, high transconductance and low drain leakage current. It has also been shown that the planar-type

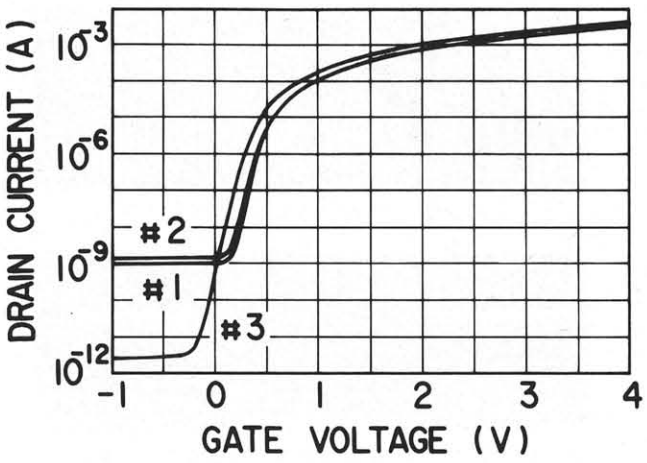


Fig. 4 Subthreshold characteristics of LID-MOSFETs with a 10-μm gate length, a 50-μm gate width, and 10-nm gate oxide thickness. The drain voltage is 3 V.

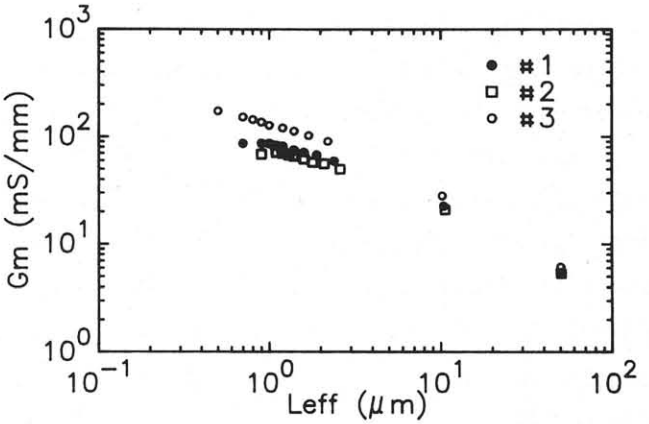
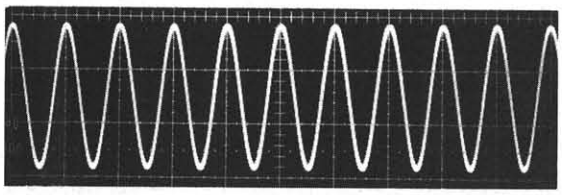


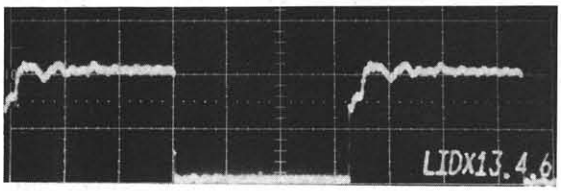
Fig. 5 Dependence of transconductance, G_m, on effective channel length, L_{eff}.

LID-MOS has nearly the same characteristics as those of the mesa type. This is significant because the planar type does not involve a troublesome high-temperature epitaxial process and because smaller gate lengths can be realized owing to the smooth surface of the source/drain polysilicon.

In order to demonstrate the feasibility of the new self-aligned LID-MOS for LSIs, an E/D MOS 1/256 frequency divider was fabricated. The implemented devices are #2-type with an L_{eff} of 0.8 μm, a driver channel width of 12 μm, and a lord channel width of 4 μm. Figure 6 shows the input and output waveforms of the frequency



(a) Input (1V, 5ns/DIV)



(b) Output (500mV, 200ns/DIV)

Fig. 6 Input and output waveforms of the LID-MOS 1/256 frequency divider, operated with f_{in} = 200 MHz, V_{DD} = 3 V, and I_{DD} = 5.1 mA.

divider, operated with a power supply of 3 V and an input frequency of 200 MHz. The net power consumption was 15.3 mW.

Note that the FETs with a high degree of self-alignment can be integrated to construct a relatively large circuit. The rather low operation frequency is mainly due to improper depletion channel doping and is not considered to be an intrinsic problem of the LID-MOSFET.

4. Conclusions

An advanced LID-MOS technology was developed to solve the problem of source/drain capacitance and series resistance in scaled devices. In the new LID-MOS technology, relative positions of gate, polysilicon source/drain diffused layer, and field insulator are exactly determined by a self-alignment method. N-channel MOSFETs with a gate oxide thickness of 10 nm and an effective channel length of 0.5 μm were fabricated and attained a maximum transconductance of 173 mS/mm and a drain leakage current of $\sim$0.1 pA/μm at V_D = 3 V. Feasibility of the self-aligned LID-MOS was successfully demonstrated by incorporating the developed devices in a 1/256 frequency divider.

Acknowledgment

The authors wish to thank T. Sakai and K. Izumi for helpful discussions. They are also indebted to H. Ikawa, H. Yoshino, S. Kuwano, H. Namatsu, Y. Utsuki, and M. Sekimoto for their support in fabricating the devices, and to K. Maehara, H. Fukuda, and K. Matsuda for circuit designing and measurement of the frequency divider.

References

1) H. Inokawa, T. Kobayashi, and K. Kiuchi: IEEE Electron Device Lett. EDL-8 (1987) 98.

2) Y. Tanabe, Y. Kobayashi, Y. Yamamoto, and T. Sakai: Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo (1987) 343.

3) T.-Y. Huang, I-W. Wu, and J.Y. Chen: IEEE Electron Device Lett. EDL-7 (1986) 314.

4) W.T. Lynch, Technical Digest of IEDM 87 (1987) 354.