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Lateral Autodoping Suppression by Selective Epitaxy Capping and Its Application in High Speed BiCMOS

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This paper describes an effective way to suppress lateral autodoping from heavily arsenic doped buried layer during silicon epitaxy. A thin epi layer is grown selectively on the buried layer. This layer suppresses the release of arsenic during the subsequent epi growth. Lightly doped p-type epi region can be grown adjacent to arsenic buried layer. This technique significantly simplifies the buried layer isolation process and minimizes the parasitic collector capacitance of the bipolar device. It has been successfully integrated into a high performance Non-OVerlapping super self-Aligned (NOVA) BiCMOS technology[1].

Introduction

The cross section of the NOVA BiCMOS is depicted in Fig.1. Bipolar and PMOS devices are fabricated within the buried layer region. NMOS are fabricated outside. The buried layer is isolated by lightly doped p-type silicon to reduce collector/substrate capacitance (C_{cs}). In the presence of lateral autodoping, the arsenic contaminant from the buried layer converts the lightly doped p-epi into n-type silicon[2]. This phenomena causes the buried layer to be shorted together in an otherwise isolated structure.

There are several approaches that can minimize lateral doping[3,4]. Antimony buried layer is known to result in very low level of autodoping[3]. However, high collector resistance due to lower antimony solubility degrades bipolar circuit performance. High temperature preepitaxial baking[2], or low pressure epitaxy deposition[4] can be used to reduce autodoping. These methods can not totally eliminate the autodoping phenomena. A practical method used in production is by forming deeply diffused p junctions to isolate the buried layers. A disadvantage is in the high C_{cs}. In addition, this region would not be suitable for NMOS device fabrication. Other advanced technique like trench isolation may be considered. Trench isolation is, however, involved and expensive.

A simple solution is to apply the recently reported selective epi growth (SEG)[4–6]. Fig.2 illustrates the process sequence. Single crystal silicon is selectively grown inside oxide windows. The highly doped buried layer is now capped. In addition, the oxide protects the off-buried layer region from the arsenic contamination. Subsequently, the oxide mask is removed and an epitaxy layer of desired doping is deposited. Lateral autodoping can be reduced by 2-3 orders of magnitude while maintaining a low arsenic buried layer sheet resistance.

Experiment

P-type wafers of 10-12 ohms-cm resistivity and (100) orientation, 2 inches in diameter, were used. Thermal oxide, 400-600nm thick, was grown. Buried layer was patterned, the oxide was wet etched, and the photoresist was stripped. Arsenic was implanted at 150keV and a dose of 3E15 cm^{-2}, and the implanted layer was annealed. Before epi deposition, the wafers were etched in

dilute HF (H_2O:HF = 100:1).

The epi was grown in a Gemini I system. After the wafers were loaded, the system was ramped up to the desired temperature. The chamber was pumped down to 100 torr. Selective epi was deposited at 950°C. The oxide was removed after selective epi growth. Unless otherwise specified, an intrinsic epi layer of 0.8-1 μm was then grown at 1050°C. The doping profiles were obtained using spreading resistance measurement technique. The conductivity type of the substrate was identified by using a hot probe in conjunction with spreading resistance. The lapped samples were stained to confirm the conductivity type.

Results

To illustrate the severity of lateral autodoping, an intrinsic epi layer was deposited over an arsenic buried layer. The wafer was first subjected to a high temperature bake at 1100°C for 10 minutes so that the surface doping concentration was lowered. The intrinsic deposition temperature was 1000°C. N-type carrier over the buried layer decayed exponentially from the buried layer-epi interface (Fig.3a). Similar carrier profile was observed on the off-buried layer region (Fig.3b). The measurement confirmed the presence of significant arsenic contamination.

Fig.4 showed the carrier profiles after selective epi capping were incorporated. Measurement indicated that the epi film over the buried layer region was n-type (Fig.4a). With a capping layer of 300nm, the epi outside of the buried-layer boundary was p-type (Fig.4b). No lateral autodoping peak was observed. We concluded that arsenic lateral autodoping must be lower than background doping.

It was expected that a thinner SEG layer would not be as effective in capping arsenic contamination. A 200nm thick SEG were tried. On the buried layer, the profile was similar to Fig.4a. Measurement of the off-buried layer showed that n-type epi layer was obtained (Fig.4c). Even though n-type doping concentration was still low, it strongly suggested the presence of arsenic lateral autodoping.

This epi growth technique has been applied to a our high performance NOVA BiCMOS technology. A p-type epi layer of 1μm thick with a carrier concentration of $10^{15}cm^{-3}$ is deposited. Because lateral autodoping was suppressed, a simple fully recessed oxide (400nm thick) with a light field implant completed the device isolation. CMOS ring oscillator delay versus channel length is plotted in Fig.5. With this epi process, an average per stage delay of 110ps at L_{eff} of 0.75μm was measured. High speed bipolar with an f_T of 12.6Ghz has been fabricated. ECL ring oscillators with a delay of 125ps/stage was obtained (Fig.6).

Discussion and Conclusion

Lateral autodoping suppressing by SEG capping have been demonstrated. We have shown that no trace of arsenic contamination was detected with a 300nm capping layer. Therefore, isolation of the buried layers by the lightly doped bulk silicon is achieved. The relatively low contamination level associated with 200nm SEG could be countered by introducing p-type dopant during the final epi deposition. Because this process retained the buried layer impurity without out-diffusion, very little arsenic dopant was lost during the epi growth. The sheet resistance was about 20 ohms/square.

Even though the autodoping outside the buried layer had been suppressed, there was still a substantial amount of vertical autodoping. This observation indicated that lateral and vertical autodoping had somewhat different mechanisms. An evaporation and re-deposition model for the lateral component, which should be suppressed by SEG capping, was consistent with our observation. The vertical component should have an additional contamination mechanism which could not be

suppressed by SEG cap. The trapping model proposed by Wong et. al. was consistent with our observation[7].

In conclusion, effective suppression of lateral autodoping by selective epitaxy capping has been demonstrated. Transistors have been fabricated within the buried layer region and outside the buried layer region. High speed super self-aligned CMOS and bipolar circuits have been successfully integrated using this epi technique.

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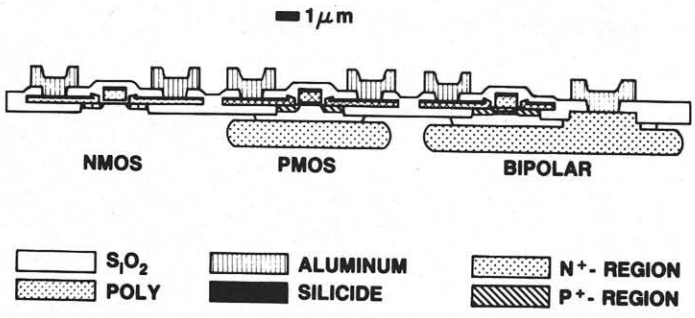


Fig. 1 The cross section of NOVA BiCMOS

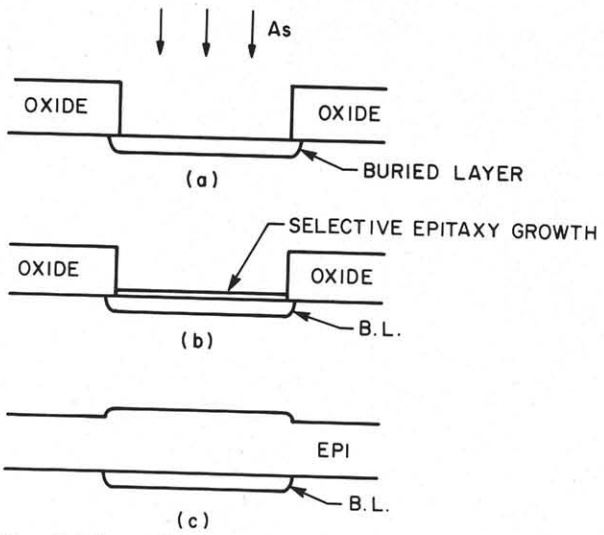


Fig. 2 The epi sequence, a) buried layer define and implant, b) SEG cap growth, c) final epi deposition

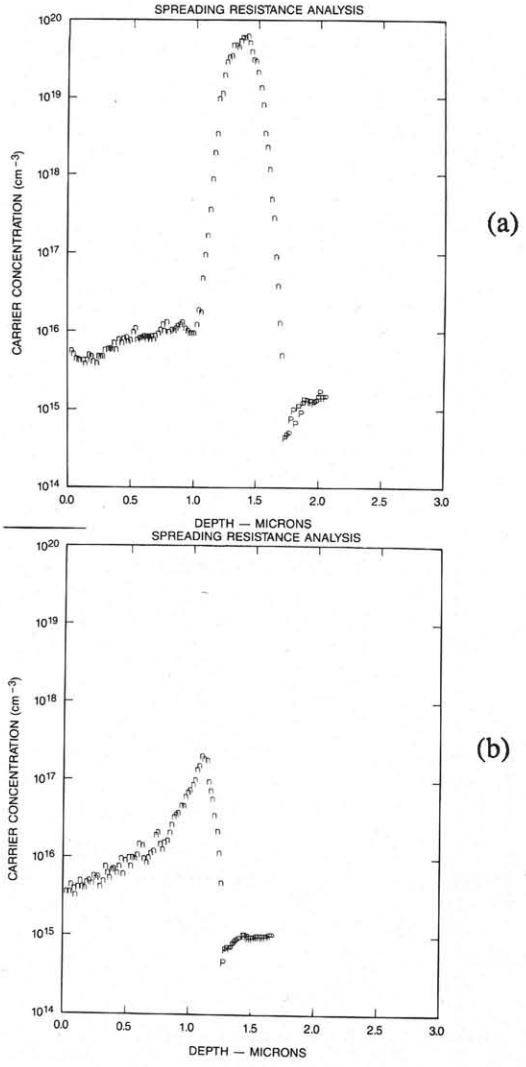
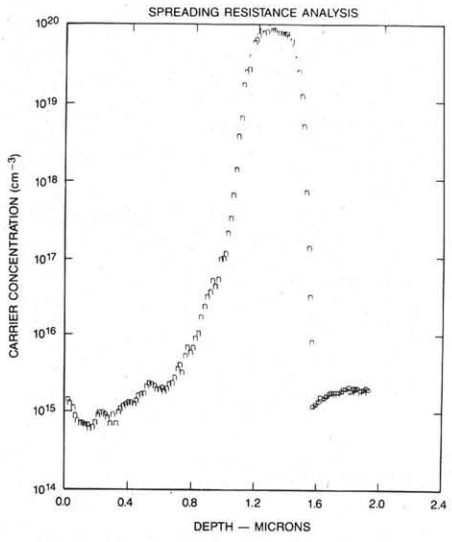
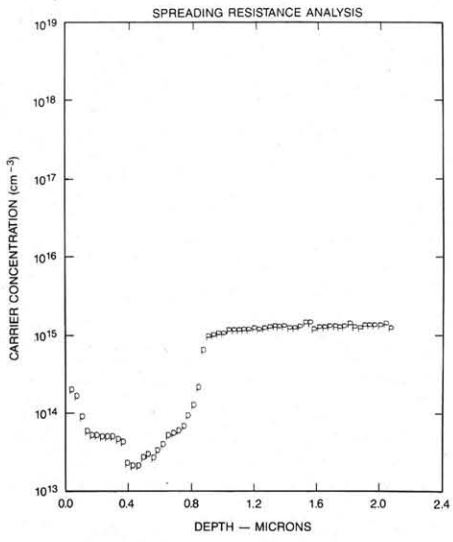


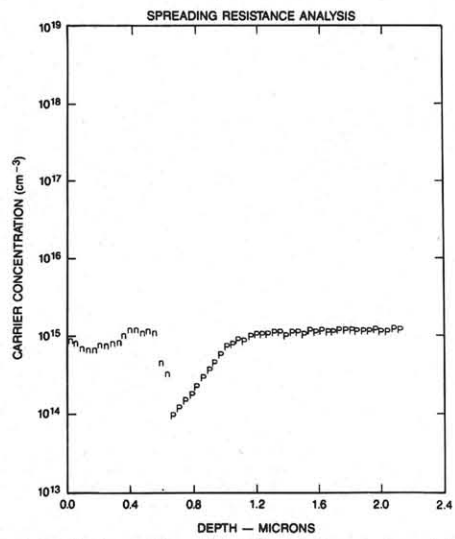
Fig. 3 The carrier profiles of epi deposited over a) buried layer and b) off-buried layer. The lettering represents the carrier type The carrier type is confirmed by using a hot probe in conjunction with spreading resistance and junction staining.



(a)



(b)



(c)

Fig. 4 The carrier profiles of epi deposited over a) buried layer and b) off-buried layer with a 300nm SEG cap. The profile over the off-buried layer with a 200nm cap is shown in c).

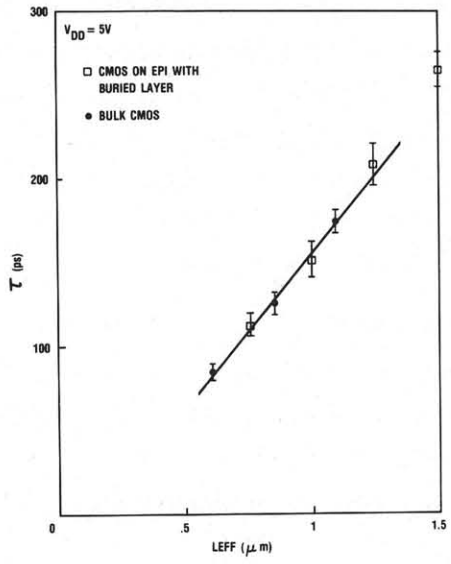


Fig. 5 The CMOS ring oscillator delay versus effective channel length. Open square are data obtained with epi substrate.

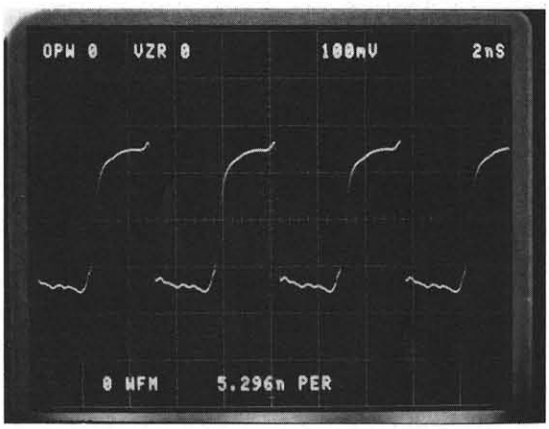


Fig. 6 Output waveform of a 21 stages ECL ring oscillator. The oscillation period is 5.3ns.