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A High Integrity and Low Resistance Ti-Polycide Gate Using a Nitrotgen Ion Implanted Buffer Layer

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A Ti-polycide gate system which has high dielectric strength and low resistivity using a nitrogen ion implanted buffer layer has been developed. The buffer layer of an approximately 30 nm thick non-stoichiometric silicon nitride is formed with N_2^+ dose below 5.0×10^{16} cm^{-2} at an acceleration energy of 15 keV. It can prevent intermixing of a Ti-silicide film and a polysilicon film, and can improve dielectric strength without increasing resistance between those films.

INTRODUCTION

A titanium disilicide-polysilicon-gate structure has enormous low-field breakdowns which are caused by the diffusion of titanium atoms into the polysilicon film. Some methods of improving dielectric strength of metal and polycide gates by using robust buffer layers such as thin LPCVD silicon nitride films are reported [1], [2], [3]. The robust buffer layer has high resistance between the metal / silicide layer and the polysilicon layer, and is not yet free from low-field breakdowns.

This paper reports a new technology of attaining high dielectric strength of a titanium disilicide-polysilicon-gate by using a nitrogen ion implanted buffer layer while maintaining its low resistivity and low resistance between the titanium disilicide layer and the polysilicon layer. The fabrication process is very simple. The new gate is expected for high speed VLSIs because of its low resistivity.

FABRICATION PROCESS

Fabrication process steps of transistors with this new gate system are shown in Fig. 1. A 200 nm thick polysilicon film was deposited on a 10 nm thick thermal silicon dioxide film grown on a silicon substrate, and a phosphorus diffusion into the polysilicon film was carried out. N_2^+ ions were implanted into the polysilicon film with doses of $1.0 \times 10^{16} \sim 1.0 \times 10^{17}$ cm^{-2} at an acceleration energy of 15 keV, to form a shallow nitrogen-rich buffer layer. A 200 nm $TiSi_{2.4}$ film was deposited by DC magnetron sputtering. A thin silicate glass film was deposited to prevent an oxidation of the $TiSi_{2.4}$ film. These films were patterned at a time by reactive ion etching to form a gate electrode. After forming conventional source/drain of p-channel MOSFETs and LDD source/drain of n-channel MOSFETs, an annealing in N_2 at 900 ~ 1000 °C for 30 ~ 60 minutes was carried out.

RESULTS and DISCUSSIONS

Transmission electron microscopy (TEM) cross-sectional micrographs of gate electrodes after an annealing at 900°C, 60min are shown in Fig. 2. Figure 2 (a) is the cross-sectional view of this gate system with N_2^+ dose 2.5×10^{16} cm^{-2},

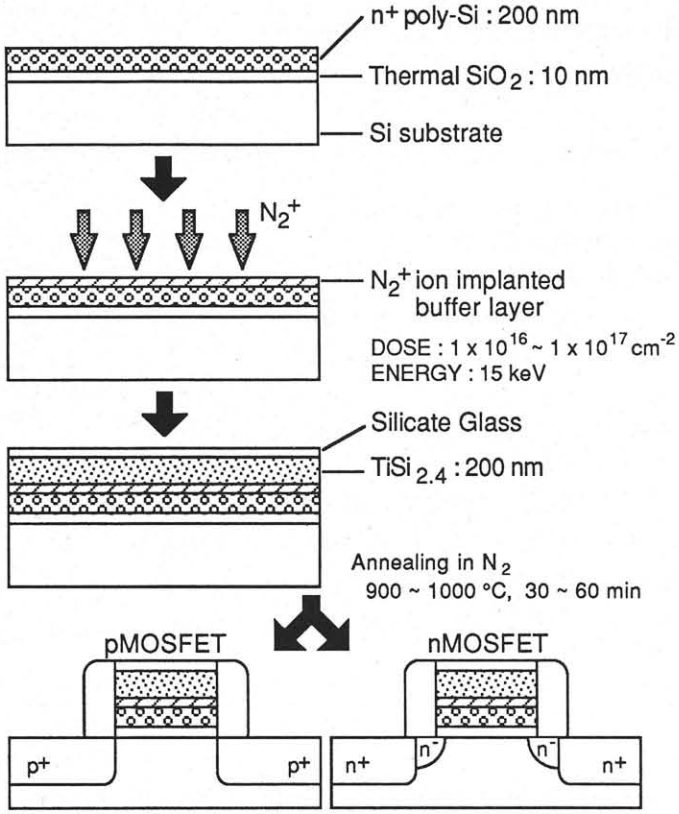

Fig. 1. Fabrication process steps of transistors with N_2^+ ion implanted Ti-polycide gate structure.

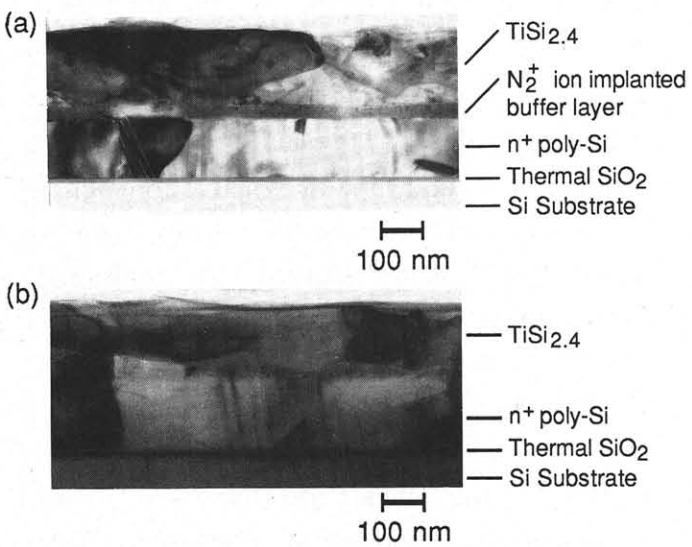

Fig. 2. TEM cross-sectional micrographs of gate electrodes after an annealing at 900 °C, 60 min, (a) with a buffer layer with N_2^+ doses of 2.5×10^{16} cm^{-2}, (b) without a buffer layer.

and Fig. 2 (b) is the cross-sectional view of a conventional polycide gate system (without a buffer layer). It was found that N_2^+ ion implantation had formed an approximately 30 nm thick buffer layer. The buffer layer was very flat and the boundaries both at a $TiSi_{2.4}$ film and a polysilicon film were very sharp. But at the conventional polycide gate system, the boundary of $TiSi_{2.4}$ film and a polysilicon film was vague.

Figure 3 (a) and (b) shows X-ray photo-electron spectroscopy (XPS) analysis of the buffer layer after the N_2 annealing with a N_2^+ dose 2.5×10^{16} cm^{-2} and 7.5×10^{16} cm^{-2} respectively. It was found that a non-stoichiometric silicon nitride (SiN_x [$x < 1.3$]) was the principal chemical state of silicon at a N_2^+ dose 2.5×10^{16} cm^{-2}. Titanium atoms were included in the buffer layer, but no titanium atom which passed through the buffer layer was observed by other XPS analysis. It was also

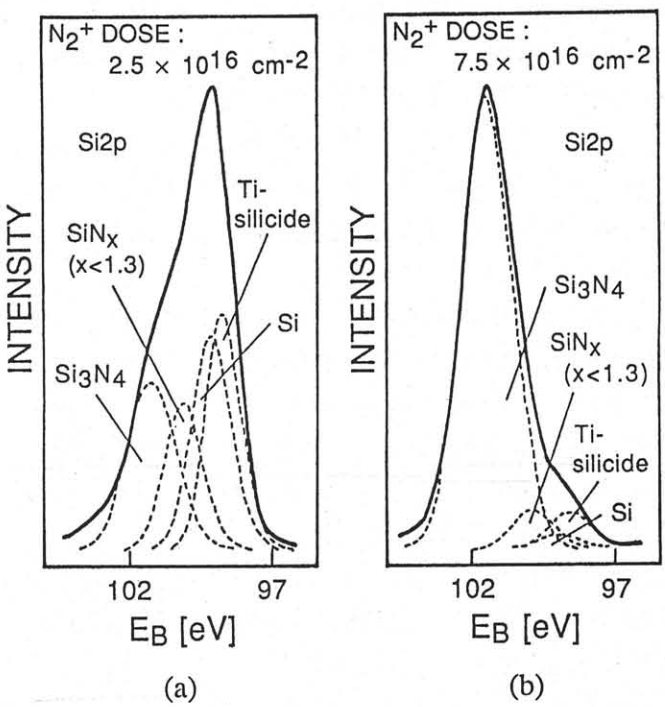

Fig. 3. XPS analysis of nitrogen ion implanted buffer layers after an annealing at 900 °C, 30 min with a N_2^+ dose, (a) 2.5×10^{16} cm^{-2}, (b) 7.5×10^{16} cm^{-2}.

found that a stoichiometric silicon nitride (Si_3N_4) was the dominant compound at a N_2^+ dose 7.5 $\times$ 10^{16} cm^{-2} and the buffer layer suppressed diffusion of titanium atoms effectively.

A comparison of dielectric breakdown characteristics of MOS capacitors between this gate system with a N_2^+ dose 2.5$\times$ 10^{16} cm^{-2} and a conventional polycide gate system are shown in Fig. 4. Figure 4 (a) shows results after annealing in N_2 at 900 °C for 60 min, and Fig. 4 (b) shows those after annealing in N_2 at 1000 °C for 60 min. The thickness of $TiSi_{2.4}$ films and that of polysilicon films were 200 nm, respectively. The thickness of the gate oxide was 10 nm, and area of the gate electrode was 10 mm^2. The breakdown characteristic of this technology had very sharp distribution and the breakdown field was higher than 8 MV/cm at 1.0 $\times$ 10^{-4} A/cm^2.

Figure 5 shows series contact resistances of 1.9 μm $\times$ 1.9 μm size between $TiSi_{2.4}$ films and polysilicon films as a function of N_2^+ dose, measured by the Kelvin method. There was no increase of the series contact resistance up to N_2^+ doses 5.0 $\times$ 10^{16} cm^{-2}. At a N_2^+ dose 7.5 $\times$ 10^{16} cm^{-2}, however, they were drastically increased because a stoichiometric silicon nitride film was formed. And sheet resistance of the gate electrode of this technology was still kept as low as 1.4 Ω/square.

As shown in Fig. 6, excellent subthreshold characteristics were obtained for both p-channel and n-channel devices with this technology of which L_{mask} were 0.8 μm. And no indication of damage by N_2^+ ion implantation was shown.

Table 1 shows propagation delay time of this gate system, measured by using 61-stages CMOS type ring oscillators. W_{mask} of p-channel MOSFETs and n-channel MOSFETs were 30 μm and 20 μm, respectively, and L_{mask} were 0.8 μm. Supplying the oscillator with 5 V, short delay time of 150 psec / stage and power dissipation of 80 μW / stage were obtained.

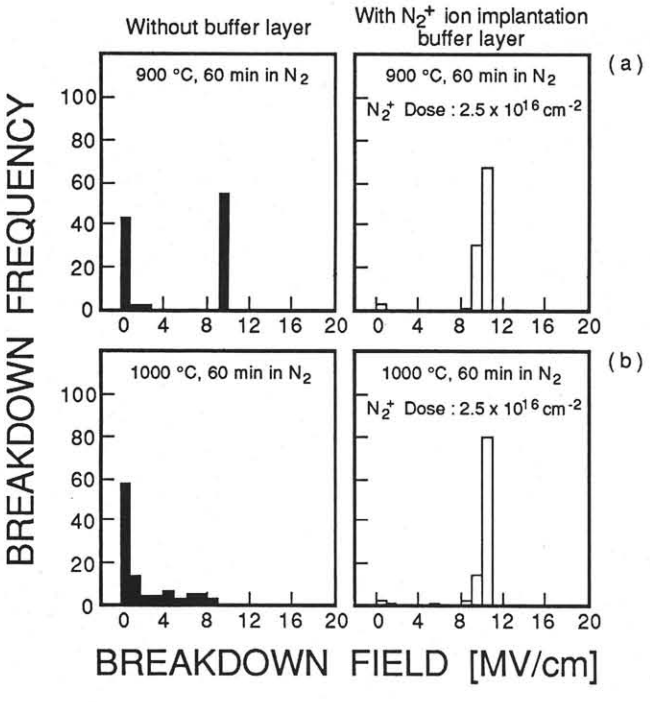

Fig. 4. Dielectric breakdown histograms of MOS capacitors (100 chips) without buffer layer gate system and with N_2^+ ion implanted buffer layer gate system, after annealing in N_2, (a) 900 °C, 60 min, (b) 1000 °C, 60 min. The thickness of $TiSi_{2.4}$ films and that of polysilicon films are 200 nm respectively, and gate area is 10 mm^2.

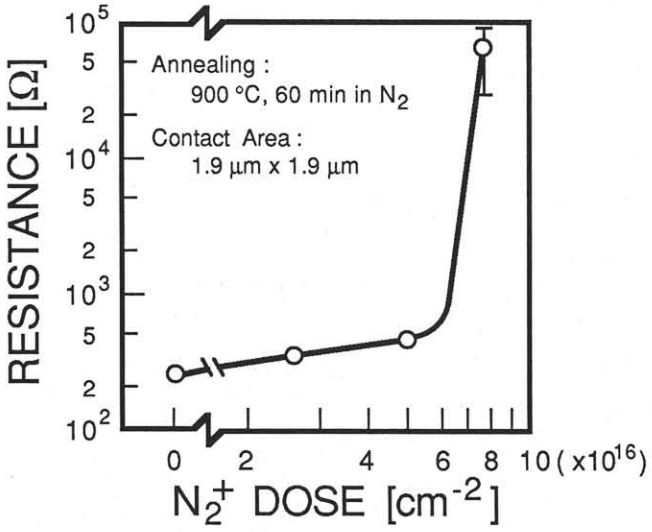

Fig. 5. Series contact resistances between $TiSi_{2.4}$ films (200 nm) and polysilicon films (200 nm) through buffer layers versus N_2^+ doses. The area of a contact hole is 1.9 μm x 1.9 μm, and annealing condition is 900 °C, 60 min in N_2.

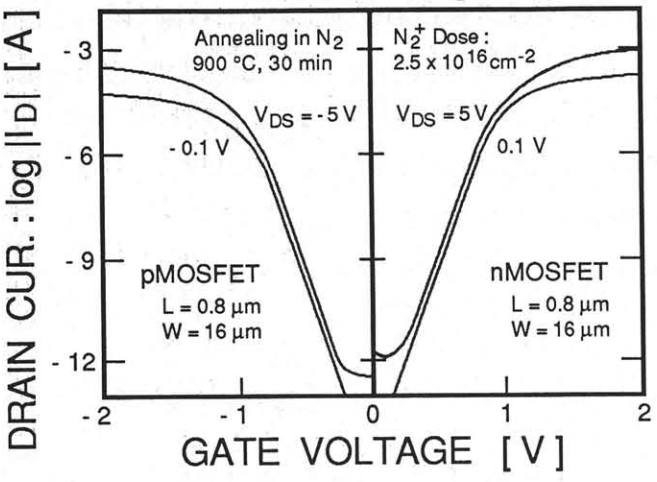

Fig. 6. Subthreshold characteristics for p-channel MOSFET and n-channel MOSFET with nitrogen ion implanted buffer layer technology. The thickness of $TiSi_{2.4}$ films and that of polysilicon films are 200 nm respectively.

Table 1 Propagation delay time of this technology measured by using 61-stages CMOS type ring oscillators fabricated using nitrogen ion implanted buffer layer technology. L_{mask} is 0.8 μm, W_{mask} of p-channel MOSFET and n-channel MOSFET are 30 μm and 20 μm respectively, and t_{ox} is 10 nm.

Gate electrode structure *	t_{pd} ** [psec / stage]	Power dissipation [μW / stage]
$TiSi_{2.4}$ / N_2^+ i/i / poly-Si (200 nm) *** (200 nm)	150	80

* Annealing in N_2 at 900°C for 30 min.
** V_{DD} : 5V
*** N_2^+ dose : 2.5 x 10^{16} cm^{-2}

CONCLUSION

The titanium disilicide film / nitrogen ion implanted buffer layer / polysilicon film gate structure for VLSIs, which can attain both high dielectric strength > 8 MV/cm and low resistivity < 1.4Ω/square, has been developed. The buffer layer can improve dielectric strength of Ti-polycide gate without increasing resistance between titanium disilicide film and polysilicon film. This structure can reduce interconnection resistance by over an order of magnitude as compared with a polysilicon gate. Consequently, this technology is expected for realizing high speed VLSI circuits.

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