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$TiSi_2$ and TiN Formation by Ti-Ion Implantation and Their Application to MOS Devices

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A 70-nm-thick, 19-$\mu\Omega$•cm titanium silicide layer has been formed using a Ti-ion implantation technique. Simultaneous formation of titanium-nitride/titanium-silicide double layers has also been performed successfully. Surface morphology of those layers was superior to that of the conventional deposition technique. Discrete pn-junction diodes and MOS capacitors were fabricated to verify the influences of Ti-ion implantation on electrical characteristics. The leakage current of the pn junction was dramatically improved using the Ti-ion implantation technique compared to the conventional deposition technique.

1. Introduction

Many kinds of silicides have been studied for the purpose of reducing parasitic resistance in MOS devices. Recently, silicidation by transition metal-ion implantation has been suggested as an alternative to silicidation by the conventional sputtering deposition[1]. The ion implantation technique is considered to be superior to the sputtering deposition technique, because the uniform reaction over the metal/silicon interface is expected. Ion implantation, moreover, is free from contamination by impurity.

In this paper, we focus on $TiSi_2$, which has the lowest resistivity among the silicides. Recently, considerable research has concentrated on developing a new metallization material to replace the conventional Al for the suppression of electromigration. This requires a barrier material beneath the metal. TiN is one such promising barrier material. We have thus investigated how to form the $TiSi_2$ and TiN films simultaneously by Ti-ion implantation. The influences of the silicidation process on electrical characteristics in pn junctions and silicon-gate MOS capacitors were also evaluated.

2. Experimental procedure

The Ti-ion beam was extracted from a microwave ion source using $TiCl_4$. The implantation into poly-Si or Si_3N_4 film and bulk silicon was performed followed by annealing at a temperature between 400℃ and 900℃. After that, the sheet resistance of the films was measured by the 4-point probe technique. Their composition and crystallinity were analyzed by AES, XPS, and x-ray diffraction.

Discrete pn-junction diodes with titanium silicide were fabricated to evaluate the influence of the silicidation process on the device characteristics and to verify the applicability to MOS devices. A (100) n- or p-type monocrystalline silicon was used as the base material. Phosphorous ions were implanted into the p-type substrate, and boron ions into the n-type substrate, followed by annealing. Ti ions were implanted at 30 keV by $1x10^{17}cm^{-2}$ into the n^+- or p^+- regions, with or without a screen Si_3N_4 film.

Poly-Si gate MOS capacitors with a gate oxide thickness of approximately 20nm were fabricated. Boron or phosphorous ions were implanted into the gate poly-Si, followed by the ion implantation with a dose of $1x10^{17}$ Ti cm^{-2} at 50 keV.

3. Properties of Ti-ion implanted layers

3.1 Characterization of Ti-ion implanted silicon

Figure 1 shows the sheet resistance of Ti-ion implanted poly-Si film. The minimum value of the sheet resistance is obtained at an annealing temperature of approximately 700℃. The resistivity of this layer is 19 $\mu\Omega$·cm. This is almost the same as the value (15 $\mu\Omega$·cm) which is obtained by the conventional Ti-sputtering deposition technique. The films' Ti and Si depth profiles, analyzed by AES, are shown in Fig. 2. It was found that the layer was mainly transformed to $TiSi_2$ by the 700℃ annealing, which is reasonable according to the thermodynamics. The phase of the Ti-ion-implanted and annealed poly-Si layer was verified by the x-ray diffraction technique, showing the dominant orthorhombic orientation [010].

Figure 3 shows a cross-sectional photograph of the Ti-ion implanted and annealed poly-Si film by TEM. In this case, the thickness of the $TiSi_2$ layer is about 70 nm. It can be seen that the interface between the silicide and poly-Si layer is very uniform. The roughness of the interface is less than 20 nm.

In a series of experiments, sheet resistance and material composition of Ti-ion implanted monocrystalline silicon were also investigated. The results were almost the same as those obtained for the poly-Si film.

3.2 Characterization of Ti-ion implanted Si_3N_4 film

The sheet resistance of the Ti-ion implanted Si_3N_4 film reaches its minimal value at the annealing temperature of approximately 700℃, as is shown in Fig. 4. At 700℃, the conductive film showed an average resistivity of about 400 $\mu\Omega$·cm over the whole implanted region. This resistivity is higher than that of the conventional sputter-deposited TiN film. According to AES and XPS analyses, the Ti-ion implanted and annealed Si_3N_4 film consists of a trilayer: that is, a superficial oxide layer, a silicon-rich layer and a nitrogen-rich layer. As was

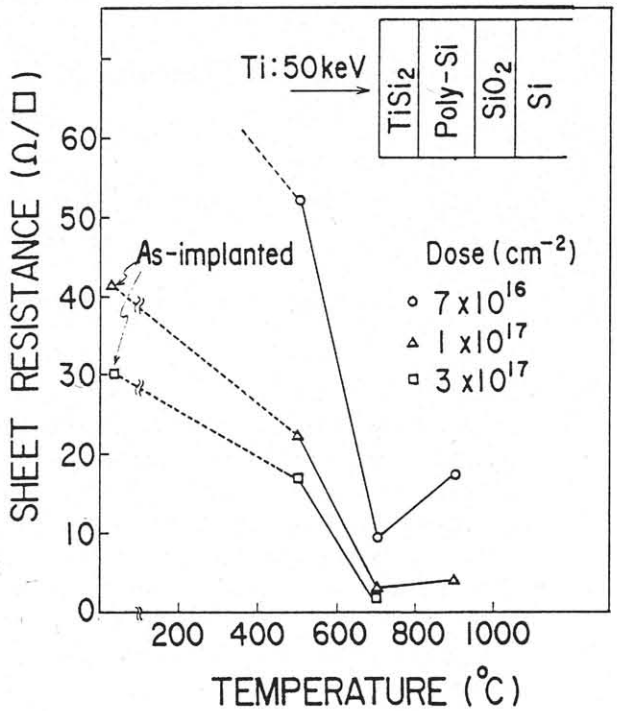

Fig.1. Sheet resistance dependency of Ti-implanted poly-Si on annealing temperature.

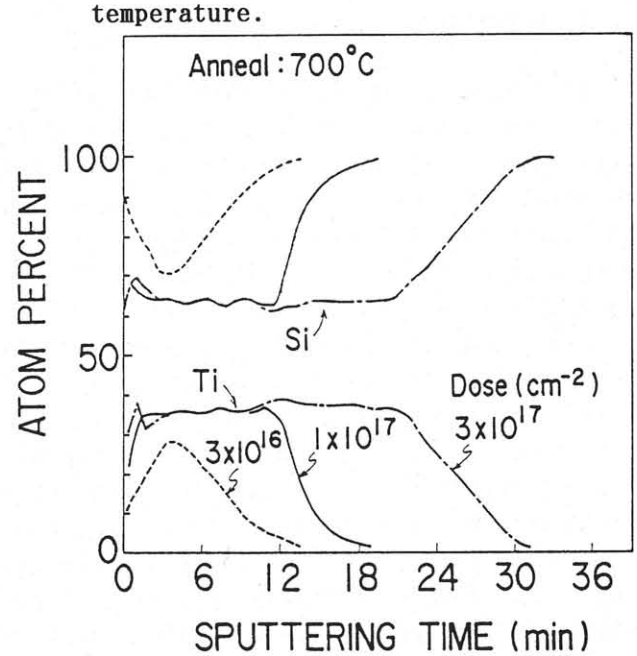

Fig.2. Ti and Si depth profiles in Ti-implanted poly-Si.

confirmed from the binding energy analysis using the XPS technique, the oxide layer included titanium oxide and silicon oxide which were formed during the annealing in nitrogen. It is considered that the somewhat high resistivity of the Ti-ion implanted Si_3N_4 layer is due to the microscopic mixture of titanium oxide and silicon oxide.

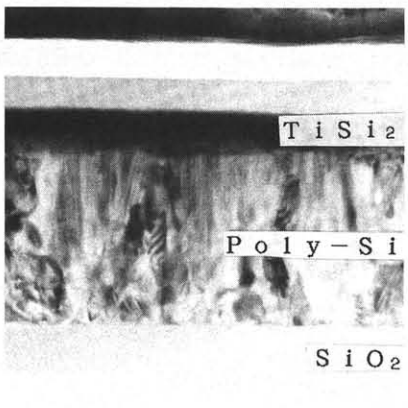

Fig.3. Cross-sectional photograph of Ti-implanted poly-Si by TEM.

3.3 Surface morphology of Ti-ion-implanted layers

Surface morphology was investigated from the perspective of applicability to device fabrication processes.

SEM photographs of the surface morphology of the Ti-ion-implanted and annealed poly-Si layer are compared with that of titanium silicide by the sputtering deposition technique and shown in Figs. 5(b) and 5(a), respectively. In these photographs, samples were tilted by 75° to emphasize the surface morphology. It is demonstrated that the morphology of the Ti-ion-implanted layer is superior to that of the conventional one. The morphology was independent of the dopants, which in this case were phosphorus, boron and arsen.

Titanium nitride/titanium silicide double layers were formed on the top of (100) monocrystalline silicon. This double layer was formed by Ti-ion implantation after a Si_3N_4 film was deposited on the monocrystalline silicon surface. A titanium-silicide single layer was also formed on (100) monocrystalline silicon for comparison. SEM photographs are shown in Figs. 5c and 5d. The surface morphology was improved drastically by providing a thin Si_3N_4 capping layer on the silicon before the Ti implantation. Here too the morphology was independent of the dopants.

4. Device application

4.1 pn-junction diodes

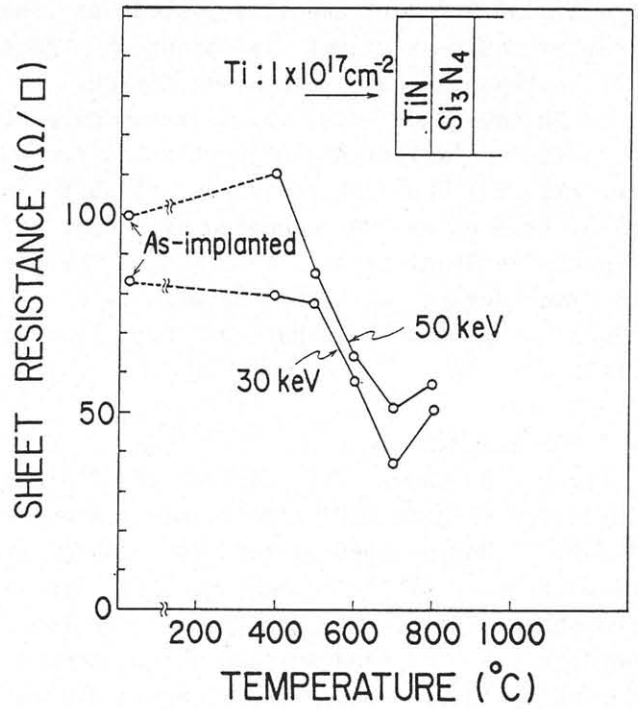

Fig.4. Sheet resistance dependency of Ti-implanted Si_3N_4 on annealing temperature.

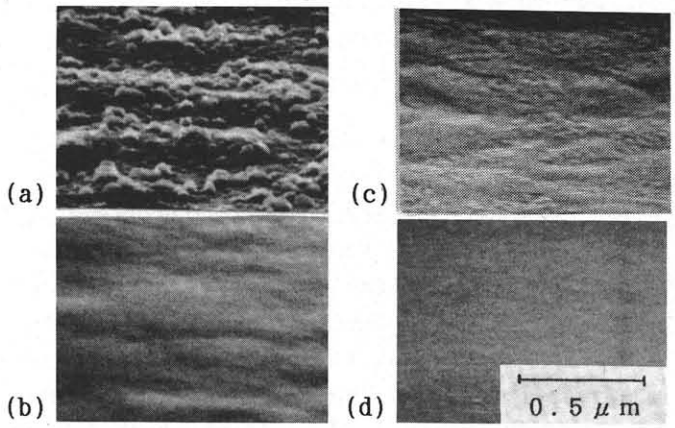

Fig.5. Surface morphology of titanium silicide surfaces. Tilt angle : 75°
(a) $TiSi_2/n^+$-poly Si by Ti deposition
(b) $TiSi_2/n^+$-poly Si by Ti implant.
(c) $TiSi_2$/(100) Si by Ti implant.
(d) $TiN/TiSi_2$/(100) Si by implant.

The reverse-biased I-V characteristics of a Ti-ion implanted n^+p junction is plotted in Fig. 6. A cross-sectional view of the device is shown as an inset in the figure. At 5 V, the leakage current of the Ti-ion implanted device was reduced by 4 orders of magnitude compared with that of the conventional silicide n^+p junction. The leakage current of the device with the $TiN/TiSi_2$ double layer formed by Ti-ion implantation has been improved by an

additional order of magnitude, although the leakage current level is about 5 times larger than that of the control device.

On the other hand, the leakage current of a Ti-ion-implanted p^+n junction is shown in Fig. 7. The leakage current at -5 V is also reduced by 70%, compared with that of the conventional type. The leakage current of the device with the double layer is almost the same as that of the control device.

4.2 MOS capacitors

Figure 8 shows C-V curves of Ti-ion-implanted Si-gate MOS capacitors measured at 1 MHz. A boron-doped Si-gate MOS capacitor is unaffected by Ti-ion implantation. In a phosphorous-doped Si-gate MOS capacitor, however, a flat-band voltage shift occurs. According to SIMS analysis, Ti atoms did not reach the gate oxide. It was confirmed by the TVS technique at 270℃ that the shift is not due to a mobile charge, but rather to a fixed charge.

5. Summary

A thin, low-resistivity titanium silicide layer has been successfully formed using a Ti-ion implantation technique. Simultaneous formation of titanium nitride/titanium silicide double layers has also been performed successfully. Surface morphology of those layers was superior to that grown by the conventional deposition technique. The leakage current of the pn junction was improved drastically by the Ti-ion implantation technique. MOS characteristics were generally stable.

Experimental results demonstrate that titanium silicide and titanium nitride formation by Ti-ion implantation is a promising technique because of its simple applicability to MOS devices.

Acknowledgment

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References

1) M. N. Kozicki,"Silicide Formation by Direct Metal Implantation," ECS Fall Meeting, Ext. Abstract No.685(1987).

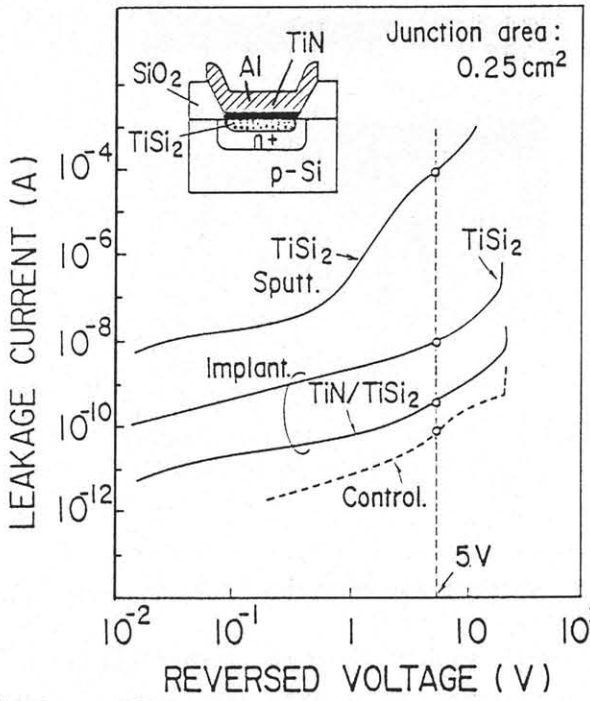

Fig.6. Leakage current characteristics of n^+p junctions with a $TiSi_2$ or TiN/TiS_2 layer.

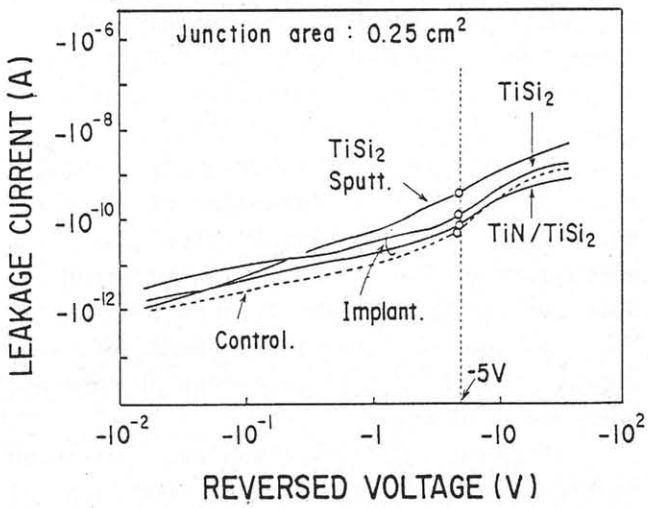

Fig.7. Leakage current characteristics of p^+n junctions with a $TiSi_2$ or TiN/TiS_2 layer.

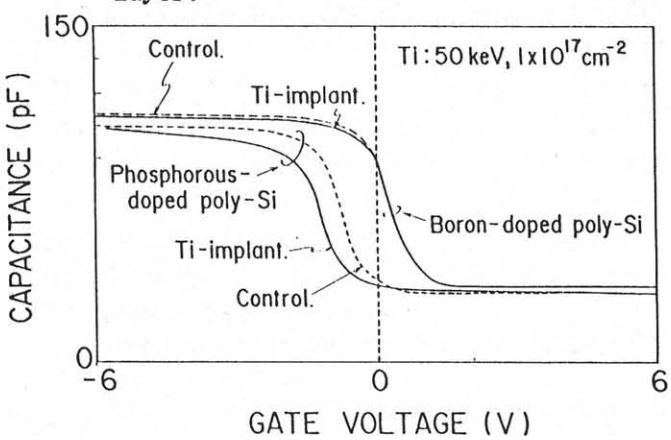

Fig.8. 1-MHz C-V curves of Ti-implanted Si-gate MOS capacitors.