

Lateral Diffusion of Dopants beyond Preamorphized Region

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A preamorphization technique with a Si-implantation was optimized in terms of both reduction of junction depth and suppression of leakage current, and was applied to the fabrication of source and drain of PMOSFETs. However, short-channel effects weren't improved as expected. Estimated 2-D profiles of an amorphized region by a Si-implant and subsequently implanted boron suggested there was a non-overlapped region under an edge of gate, which allows the dopants to spread laterally through channeling. The phenomenon was confirmed by preamorphization with a Si-implantation of tilted incidence.

1. INTRODUCTION

A preamorphization technique with a Si-implantation¹⁻³⁾ has been studied to eliminate an ion-channeling tail of boron for the formation of shallow p⁺/n junction. Residual defects caused by Si-implantation are hard to be annealed out completely by subsequent thermal processes. Therefore, on application of the technique to the formation of source and drain of PMOSFETs, the depth of an amorphized region and implanted boron must be properly adjusted not to leave the defects remaining in channel regions and depletion layers, because they act as generation-recombination centers.

In addition, it has been clarified that only optimization in terms of the "depth" is not enough to achieve quarter-micron devices. In this paper, lateral diffusion of boron beyond the preamorphized region at an edge of gate is discussed.

2. p⁺/n DIODE FABRICATION

p⁺/n Diodes were fabricated first in order to obtain optimized conditions of the preamorphization technique in terms of junction depth and leakage current due to residual defects. Si-ions were implanted to 2×10^{15} cm⁻² at 40 keV, and then BF₂-ions were implanted to 2×10^{15} cm⁻² at 5 or 30 keV. Boron was activated by RTA (Rapid Thermal Annealing) at 800 °C or 1000 °C for 10 sec. Junction depth was measured by angle-lapping-staining techniques and the leakage current was measured at -2.5 V. The results are summarized in Table 1 and the junction depth was reduced by about 70 nm for a BF₂-implant at 30 keV and 1000 °C RTA by preamorphization with a Si-implant.

3. "OPTIMIZED" FABRICATION OF PMOSFETS

If lateral spreads of boron-ions are assumed to be suppressed as much as the reduction of junction depth, effective channel length of MOSFETs is expected to be longer by about twice of the reduction of junction depth due to contribu-

Table 1 Effects of preamorphization on junction depth x_j and leakage current J_R .

			RTA (10 sec)			
			800 °C		1000 °C	
			NO SI-IMPLANT	SI-IMPLANT	NO SI-IMPLANT	SI-IMPLANT
BF ₂ ⁺ (2E15 cm ⁻²)	5 keV	x_j (nm) J_R (A·cm ⁻²)				50 1.8E-8
	30 keV	x_j (nm) J_R (A·cm ⁻²)	200 9.6E-9	100 6.6E-6	200 5.0E-9	130 1.8E-9

SI-IMPLANT : 2E15 cm⁻², 40 keV V_R : 2.5 V

tions from both sides of source and drain. Increments of electrical effective channel length were studied for the MOSFETs fabricated with the optimized condition of a Si-implantation obtained above. The MOSFETs had gate defined by EB-direct-writing and deviation of the length was about 30 nm. The result is shown in Fig.1. Though the junction depth reduced as the energy of BF₂-ions was decreased, the expected reduction was not observed at 25 keV. This result was contrary to that obtained in the diodes previously mentioned. If BF₂-ions are implanted at a lower energy than 25 keV, leakage current is observed as shown in Fig.2. Therefore, suppression of both leakage current and channeling seems to be a trade-off.

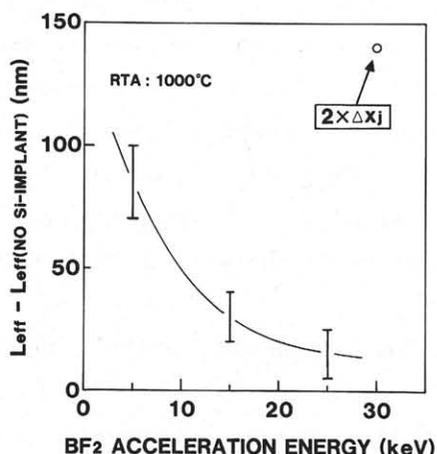


Fig.1 Dependence of increments of effective channel length on BF₂-ion energy. An open circle indicates twice of the reduction of junction depth.

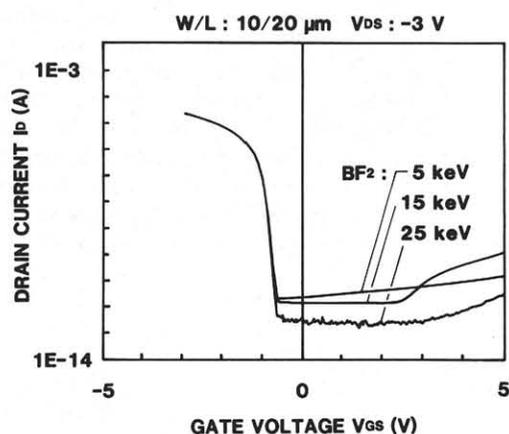


Fig.2 I_D - V_G characteristics of PMOSFETs with a Si-implant.

4. ESTIMATION OF 2-D PROFILES

Two-dimensional spreads of the amorphized region and a boron profile under an edge of gate was estimated. The amorphized region was defined as a region whose energy density given by atomic collisions exceeded the critical energy⁴⁾ of 6×10^{23} eV·cm⁻³ and the boron profile was assumed to be a Gaussian distribution. The result suggested there was a non-overlapped region of the boron profile to the amorphized region, and channeling might not be suppressed enough. It allows the dopants to spread laterally beyond the calculated profile illustrated in Fig.3(a).

5. SI-IMPLANT WITH TILTED INCIDENCE

The phenomenon suggested above was confirmed by a Si-implantation performed with tilted incidence on both sides of source and drain of MOSFETs

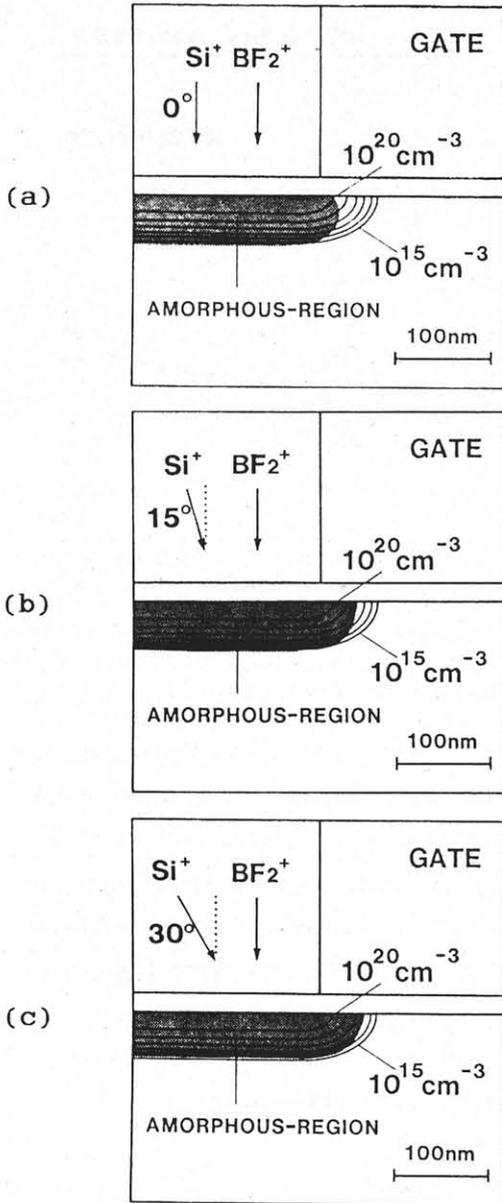


Fig.3 Estimated regions amorphized by Si-implants and boron profiles assumed a Gaussian distribution; the ions were assumed not to occur channeling. Si-ions were implanted with incident angle of (a) 0° , (b) 15° , and (c) 30° .

to fully amorphize the region under gate. The expected regions amorphized by the tilted incidence of 15° and 30° of Si-ions were illustrated in Fig.3(b) and (c) respectively. The fabrication process of the MOSFETs is described below.

Active regions of transistors were defined by conventional LOCOS process. After 20-nm thick gate oxides were grown, a surface implant was performed with

BF_2 -ions to a dose of $1.5 \times 10^{13} \text{ cm}^{-2}$ at 25 keV, and As-ions to $6 \times 10^{12} \text{ cm}^{-2}$ at 25 keV and P-ions to $3 \times 10^{12} \text{ cm}^{-2}$ at 170 keV were implanted to form punch-through stoppers. Gate-electrodes were made of n^+ -polysilicon, and defined by EB-direct-writing. Then the Si-implantation was performed with a tilted incidence of 15° , 30° , or 45° measured from normal of wafers toward source or drain, to a dose of $2 \times 10^{15} \text{ cm}^{-2}$ at 40 keV on both sides of gate; a dose was corrected for each angle. Then BF_2 -ions were implanted to $2 \times 10^{15} \text{ cm}^{-2}$ at 15 or 25 keV and were activated by RTA at 1000°C for 5 sec.

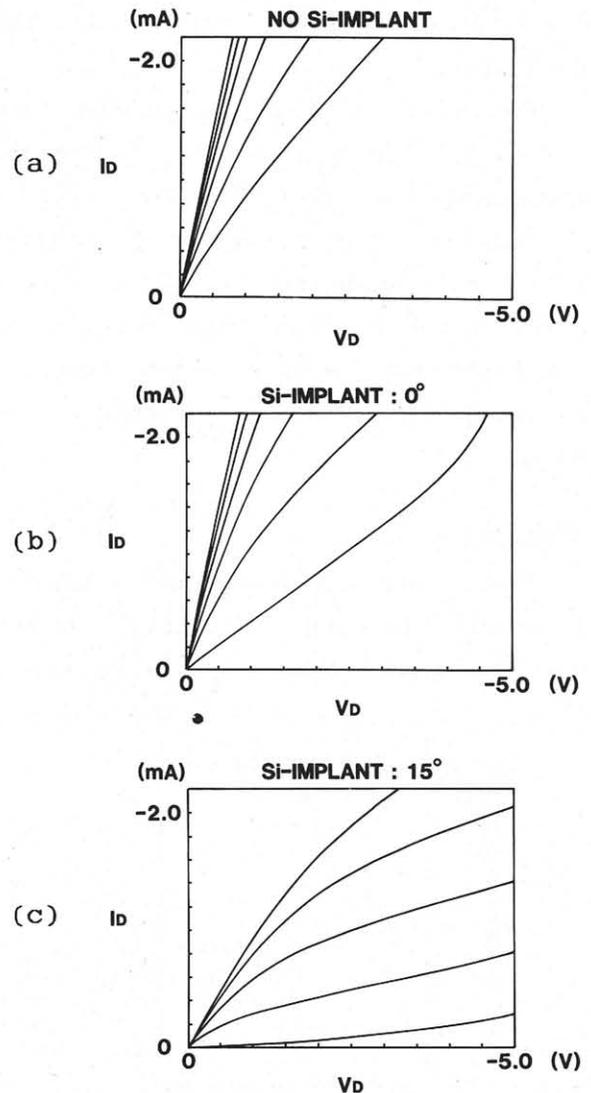


Fig.4 I_D - V_D characteristics of PMOSFETs (a) without a Si-implant, (b) with Si-implants of incident angles of 0° and (c) 15° . $L_{\text{gate}} : 0.35 \text{ um}$, $V_G : 0 \text{ to } 5 \text{ V}$, $V_{\text{sub}} : 2.5 \text{ V}$.

I_D - V_D characteristics of finished devices were shown in Fig.4. All devices shown here have 0.35- μm long gate. The Si-implantation with tilted incidence made much improvement in punch-through vulnerability. Electrical effective channel length was measured for each implantation condition and Fig.5 shows increases of the channel length over no Si-implanted samples. The maximum increase of about 0.2 μm was observed at 15° incidence of Si-ions for 25 keV of BF_2 -ions. The reduction of effective channel length for larger angles than 15° might be explained by enhanced diffusion⁵⁾ due to defects created by the Si-implantation.

Threshold voltage dependence on gate length is shown in Fig.6. Remarkable improvements of short-channel effects were observed for Si-implanted samples with tilted incidence. Inverse short-channel effects⁶⁾ seen here are due to a punch-through stopper which forms a non-uniform impurity concentration profile.

6. CONCLUSION

It has been confirmed that a profile of dopants spreads laterally through channeling beyond because of a non-over-

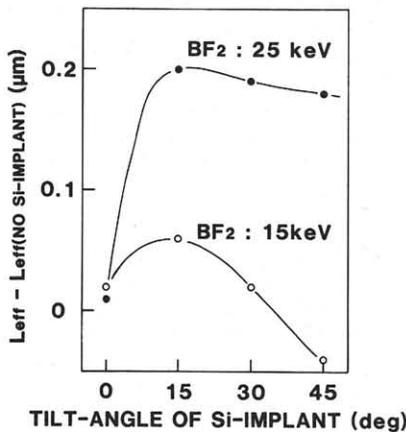


Fig.5 Increments of effective channel length as a function of Incident angles of Si-implants.

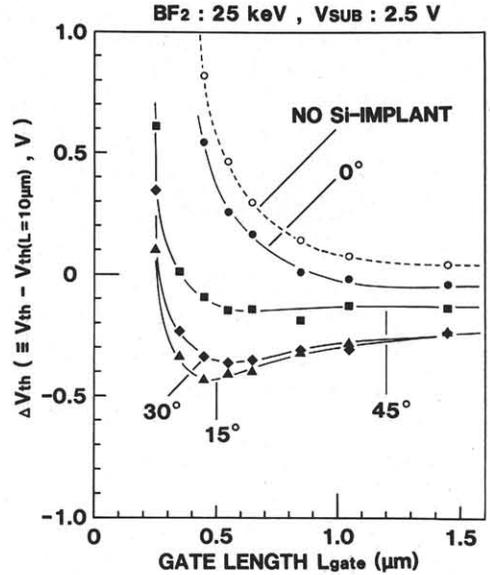


Fig.6 Channel length dependence of threshold voltage for various incident angles of Si-implants.

lapped region of a dopant profile to an amorphized region at a mask edge even if their depth is optimized. Therefore, preamorphization conditions should be optimized in terms of two-dimensional profiles, and it can also be concluded the preamorphization technique using tilted incidence of Si-ions is effective to suppress the phenomenon.

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