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Excimer Laser Doping for Sub-Micron Device Fabrication

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A new doping process using excimer laser (Laser Induced Melting of Predeposited Impurity Doping=LIMPID) is applied to fabricate sub-micron CMOS super thin film transistor. This low temperature doping process is suited for producing a shallow junction with less side diffusion. The resultant devices (L=0.8µm) showed an excellent I-V characteristic.

1. INTRODUCTION

As devices become smaller, two problems in doping process on source-drain regions of MOSFETs have become apparent. There is a problem with side diffusion of dopants into channel region from the source-drain region. A 0.1µm to 0.2µm of a total encroaching length induced by conventional doping process consisting of ion implantation and high temperature annealing process is not negligible for a short channel devices such as 0.8µm or less. There is also a problem in that very small and deep contact holes are difficult to open and to fill with electrode materials. A 0.3µm of poly-Si gate thickness is required in an ion implantation process to stop all ions in the gate electrode. A thick gate electrode requires a thick insulating layer over it and deep contact holes.

We have previously reported a new doping method using an excimer laser to give high dose doping called Laser Induced Melting Predeposited Impurity Doping (LIMPID)¹. This doping process does not need an ion implantation or high temperature annealing. It has a potential to solve these problems mentioned above. A similar technique has already been reported by Carey et.al. using Gas Immersion Laser Doping (GILD) for making NMOS². We made sub-micron CMOS Superthin Film poly-Si Transistor (SFT)³ to demonstrate its feasibility for sub-micron device fabrication.

2. PROCESS

5-inch size Si wafers were used as a substrate. 500nm thick oxide was grown thermally at 900°C, and 150nm thick poly-Si film was deposited by low pressure chemical vapor deposition (LPCVD). The poly-Si film was then amorphousized by two steps Si ion implantation at 30keV with 1x10¹⁵dose and 75keV with 5x10¹⁵dose and annealed at 600°C for 100 hours for its grain growth and thinned to 75nm. Then the poly-Si film was patterned into small islands for each FETs and 30nm thick of gate oxide film was grown thermally over them. 100nm thick poly-Si with no dopants was deposited by LPCVD as a gate material. This thickness was determined by computer simulation. The computer simulation predicted that a thinner film of

gate poly-Si than 100nm reaches higher temperature than source-drain region with the laser irradiation, and to the contrary, a thicker film reaches lower temperature. Then the poly-Si film was patterned and the thin oxide films over source-drain regions were etched off.



SiO₂ 500nm

Si sub.

Fig. 1 A schematic cross section of SFT and illustration of LIMPID process.

The LIMPID process was carried out in a specially designed chamber which is equipped with a plasma CVD system for dopant film deposition and a large quartz window for laser irradiation. A schematic illustration of the LIPMID process is shown in figure 1. The LIMPID process consists of two steps dopant-film deposition and laser irradiation. A phosphorus film and a boron film were deposited in a glow discharge of PH3 and B2H6 diluted with Ar qas to 18. gases respectively. A thickness of the dopant film was ranged from 10nm to 20nm, it was measured by Taly Step of Taylor Hobson. A focused laser beam size on a sample surface is about 2mmx5mm. A pulsed excimer laser beam was scanned over the sample with intensities from 0.5J/cm² to 0.7J/cm² and at 20pulses per The scan speed was 2mm/s and the second. length of the beam in scanning direction was scanning irradiation Under this 2mm .

condition, 20 pulses were irradiated on one point. For CMOS fabrication, the LIMPID process was done twice for each wafer; first time for phosphorus doping for n-ch devices area whereas p-ch devices area were covered with 100nm SiO₂ film and second time for boron doping, vice versa.

After this doping process, an insulating film SiO₂ of 500nm thick was deposited by CVD and contact holes were etched. A contact metallization with Al of lµm thick was deposited by evaporation.

3.RESULTS and DISCUSSIONS

An excimer laser beam has a high energy density (up to 2J/cm² for focused area of 10mm²), a short pulse (30ns), and short wavelength (308nm for XeCl). This laser beam can melt a very thin surface (50nm to 300nm) of Si wafer or film for a very short time (50ns to 300ns), without substrate heating. When the laser beam is irradiated on Si surface on which a dopant film was predeposited, a dopant atoms were taken into the molten Si region and after the resolidification a doped layer is formed.

The diffusion coefficient of P and B are very large in the molten Si (on the order of $10^{-4} \text{cm}^2/\text{s})^4$, so that the dopant can spread entire molten region in a short time of one pulse⁴. So the junction depth is controlled by changing the laser energy. There is a dramatic change in diffusion coefficient of dopant atoms between in solid phase and in Dopant atoms do not have a liquid phase. chance to diffuse out of molten region in This means the dopants such a short time. distribute uniformly in molten region and no atom comes out, and are frozen in the network of Si lattice with resolidification of the molten Si, and are completely activated. This LIMPID process offers a very shallow doped layer (less than 0.2µm) with high concentration (about 2x10²¹/cm³) of dopants which are entirely activated. And also in this method, a same dopant is doped into the gate region as in the source-drain region, so the resultant devices have n^+ poly-Si gate electrodes for n-ch device and p^+ poly-Si for p-ch device. This symmetrical device structure can give a symmetrical electric characteristics.

In order to observe the junction depth, we applied the LIMPID on a bear Si substrate directly and measured the variation of it as a function of the energy. The dopant profiles were observed by spreading resistance measurements. 4 profiles are shown in figure 2. The junction depth varies from 50nm to 180nm with a laser energy from $0.6J/cm^2$ to $0.85J/cm^2$, but the highest dopant concentration in each profile are kept in a small $1.3 \times 10^{20} / \text{cm}^3$ range from to $2.0 \times 10^{20} / \text{cm}^3$. A similar process technique



energy.

GILD has already been reported². In the GILD process, dopant atoms are mainly supplied from gas phase, a concentration of dopant is small (about 2x10¹⁹/cm³) with one pulse. The LIMPID technique uses a dopant film as its source, so that a high concentration such as 2x10²¹/cm³ can be achieved with one pulse⁵. In the LIMPID process, the predeposited dopant film disappears after the first pulse for energy higher than 0.5J/cm², the dopant concentration in doped region does not increase much with additional pulses, but the second and latter pulses redistribute the dopant in molten region and the dopant profile finally reaches a square shape (details of this doping mechanism is discussed in reference 4).

In figure 3, we show Id versus Vq characteristics of both types MOSFET. The carrier mobilities of n-ch an p-ch are 30cm²/Vs and 25 cm²/Vs, respectively. The threshold voltages of n-ch and p-ch are 0.23V and 0.29V respectively. The irradiated laser power was 0.65J/cm² for these devices. We can notice that the off current are relatively high. This effect is now under studying, but may be due to the damage induced by twice laser irradiation for CMOS



W/L:10/0.8(µm)

Fig. 3 Id vs Vg curves of p-ch and n-ch devices.

fabrication. In figure 4, we show the Id vs Vg curve of p-ch device which was made in single step process i.e. the laser irradiation was done only once. We can see a very low off current as low as lpA. For CMOS fabrication, a SiO2 film was used as a cover to protect p-ch devices or n-ch devices from phosphorus or boron, respectively, and worked reflection film for an anti laser as So, we can reduce the off irradiation. current to lpA by employing Al films as the cover or a projection technique by putting photo masks between the wafer and the laser.





The use of thin gate material (100nm of poly-Si) is succeeded. This thinness of gate material is very difficult for conventional doping process, because an implanted atom has enough energy to penetrate through the thin gate and reaches to the channel region. A doping in gate region is also done at same time when source-drain region were doped by the LIMPID. The sheet registivity of this gate poly-Si was 2000hm/sq. with 0.6J/cm² of laser energy. This thinness of gate material may be helpful to have a thin insulating material over it and shallower contact hole.

4. CONCLUSION

We have demonstrated the feasibility of the LIMPID process for sub-micron CMOS This low temperature doping fabrication. process produced highly doped region with shallow junction and low resistivity which were evaluated by spreading resistance measurement. The CMOSFET fabricated with LIMPID showed this process excellent electrical characteristc.

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