Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 129-132

A-9-2

A 5 Gb/s 4 Bit Shift Register with 0.5 μm WNx-gate GaAs MESFETs

K.Ishida, T.Matsunaga, S.Miyano, A.Kameyama and N.Toyoda

ULSI Research Center, Toshiba Corporation

1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, JAPAN

A GaAs 4-bit shift register operating up to 5 Gb/s has been successfully developed as one of the important elements in future high-speed digital communication systems and measuring instruments. It was fabricated using a 0.5 μm WNx-gate buried p-layer LDD (BP-LDD) self-aligned GaAs MESFET process and a source coupled FET logic (SCFL) circuit. The k-value (4.80 $mA/V^2$10μm) for the 0.5 μm gate BP-LDD structured FET was 2.7 times as large as that for a 1.0 μm gate LDD structured FET. The maximum operating frequency was 2.3 times as fast as that for a 1.0 μm gate LDD structured FET.

INTRODUCTION

GaAs digital ICs have become increasingly important in high-speed digital communication systems and measuring instruments. In this application field, a Gb/s shift register is one of the leading devices. The fastest shift register reported to date operated at a clock frequency of up to 3.0 GHz [1]. In order to achieve higher speed operation, it is necessary to increase the transconductance (gm) and reduce the gate capacitance (Cgs) of the GaAs MESFETs.

In this paper, a GaAs 4-bit shift register operating at 5 GHz is presented for the first time. It was fabricated using a 0.5 μm WNx-gate buried p-layer LDD (BP-LDD) self-aligned GaAs MESFET process and an SCFL circuit. In addition, the effects of gate length shrinkage on high-speed operation is discussed.

CIRCUIT DESIGN

Figure 1 shows a block diagram of the 4-bit shift register, which is composed of four master-slave D-type flip-flops with a 3-input NOR gate, and input buffer and output buffer circuits. The input/output interfaces and supply voltage were designed to be ECL-compatible.

The basic circuit is an SCFL (source coupled FET logic [2]), as shown in Fig.2. The key points in design for the circuit parameters are the optimization of the logic swing voltage (ΔV), while maintaining a required noise margin (Vnm), and of the FET threshold voltage (Vth). The logic swing voltage (ΔV) is given by

$$\Delta V = Vgs + Vnm - Vth = R_L \cdot I_S \quad (1)$$

where Vgs is the gate-source voltage, R_L is the load resistor and I_S is the sink current. In the authors' design, both values of Vgs and Vnm were determined to be 0.35 V. The FET threshold voltage was chosen as -0.2 V. The logic swing voltage of 0.9 V was determined from Eq.(1). The load resistor of 510 ohms was designed for the sink current value I_S=1.8 mA (Wg=18 μm).

FABRICATION PROCESS

The 4-bit shift register was fabricated using BP-LDD structured 0.5 μm WNx-gate GaAs MESFETs with a shallow n-channel layer. Figure 3 shows a cross-sectional view of a 0.5 μm BP-LDD self-aligned GaAs MESFET.

An n-channel layer was formed by Si ion-implantation at 25 KeV with a dose of $7x10^{12}$ cm^{-2} into undoped semi-insulating 3-inch diameter LEC GaAs wafers. The buried p-layer was formed by Mg ion-implantation at 180 KeV with a dose of $2.5x10^{12}$ cm^{-2}. Post-implantation annealing was performed at 820 °C for 20 min in an $Ar+AsH_3$ mixed atmosphere without any encapsulating film. The WNx film was deposited by reactive RF magnetron sputtering in an $Ar+N_2$ mixed gas. The 0.5 μm gate lithography was delineated by an electron beam. The source/drain n' and n^+ layers were formed by Si ion-implantation at 45 KeV with a dose of $1.3x10^{13}$ cm^{-2} and at 105 KeV with a dose of $5x10^{13}$ cm^{-2}, respectively. The n^+ region was separated from the gate metal by a 0.3 μm long side wall. And a load resistor layer was formed by Si ion-implantation at 130 KeV with a dose of $2.6x10^{13}$ cm^{-2}.

RESULTS & DISCUSSION

FET characteristics

Figure 4(a) shows the Vth shift as a function of the gate length in the BP-LDD structured FET, compared with the conventional LDD structured FET [3]. Open circles correspond to the Vth shift for the LDD structured FET formed by Si^+ implantation at 45 KeV for the n-channel layer, without a p-layer. The closed circles are for the BP-LDD structured FET with a 25 KeV n-channel layer. In the conventional LDD structured FET, the Vth shift started at around 0.8 μm gate length, and reached 450 mV at 0.5 μm gate length. On the other hand, the Vth shift in the BP-LDD structured FET was as small as 100 mV even at 0.5 μm gate length.

Figure 4(b) shows the dependence of the K-value on the gate length. As shown in this figure, the short-channel effect was sufficiently suppressed at the gate length of 0.5 μm, and a high K-value of 4.80 $mA/V^2$10um was obtained. This value was 2.7 times as large as that of a 1.0 μm LDD structured FET. The transconductance (gm) was typically 410 mS/mm at Vth=-0.1 V, Vds=1 V and Vgs=0.4 V.

SCFL circuit performance

In order to evaluate the basic performance of the SCFL circuit, several test devices were constructed on the chip. The propagation delay time and toggle frequency were measured by using 15-stage ring oscillators and 1/4 dividers, respectively. The propagation delay time was typically 30 psec/gate at 33 mW/gate power dissipation (Vss=-5.2 V).

The 1/4 divider, which was constructed from two T-type flip-flops, operated at 11.3 GHz toggle frequency (Ftog). It was measured at the designed bias condition (Vcs=0.7 V, Vss=-5.2 V) on the wafer. The Ftog, as a function of power dissipation (Pd) for one T-F/F, is shown in Fig.5, compared with that of a 1.0 μm gate conventional LDD structured FET. A 35 % reduction in Pd/Ftog and a 2.5 times high speed in Ftog were attained for the divider with a 0.5 μm gate BP-LDD structured FET.

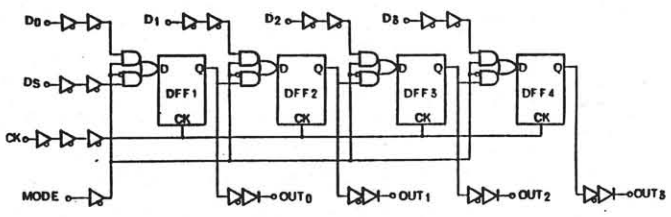
4-bit shift register performance

High-speed testing was performed directly on the wafer using a 50 ohm measurement system. Figure 6 shows an output (OUT3) waveform at 5 GHz clock frequency for the serial input mode, where the input data pattern was "0101101001010100". The power dissipation was 2 W including the I/O interface

circuits (Vss=-5.2 V).

Figure 7 shows the input bias margin characteristic for the 4-bit shift register. The horizontal axis shows the input clock frequency (Fck), and the vertical axis shows the input clock bias level (Vcb) for an input amplitude of 0.9 V. It was found that this device operated up to 5 GHz clock frequency, which was limited by the maximum frequency of the data generator being commercially available at present. This figure shows that this IC can guarantee up to 4.5 GHz in the case of a ±150 mV bias margin for the ECL input bias level (Vcb=-1.3 V).

The maximum operating frequency (Fmax) of the 4-bit shift register and Ftog of the 1/4 divider were compared with those of a 1.0 μm gate conventional LDD structured FET. The dependence of Ftog and Fmax on gate length are shown in Fig.8. The Fmax for 0.5 μm gate length, which was estimated by extrapolating in Fig.7, was 2.3 times as fast as that for 1.0 μm gate length. And the constant ratio of Fmax to Ftog was roughly 0.5:1, up to 0.5 μm gate length. A still faster operation should be possible by shrinking the gate length to the quarter micrometer region. For 0.25 μm, Fmax of 10 GHz and 20 GHz Ftog can be expected.



MODE	FUNCTION
HIGH	PARALLEL
LOW	SERIAL

Fig.1 Block diagram of 4-bit shift register

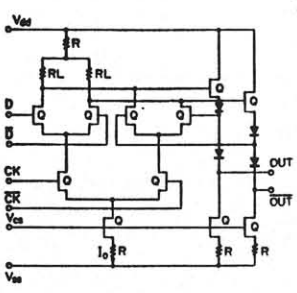


Fig.2 D-type latch circuit with SCFL

CONCLUSIONS

A GaAs 4-bit shift register for giga-bit rate digital commumication systems and high speed measuring instruments has been successfully fabricated by adopting 0.5 μm WNx-gate buried p-layer (BP) LDD GaAs MESFETs. A 5 GHz clock frequency operation was achieved at a power dissipation of 2 W.

In this paper,the effects of gate length shrinkage on high-speed operation have been discussed. The toggle frequency (Ftog) of the 1/4 divider and the maximum operating frequency (Fmax) of the shift register with a 0.5 μm BP-LDD structured FET were 2.5 times and 2.3 times as fast as those of a 1.0 μm gate LDD structured FET, respectively. An Fmax of 10 GHz and 20 GHz Ftog can be expected for quarter micrometers.

ACKNOWLEDGMENTS

The authors wish to thank Drs. H.Iizuka and H.Tango for their encouragement. They would also like to thank Messrs. S.Shimizu, N.Koide and H.Wakimoto for helpful discussions. They are also grateful to Messrs. T.Baba, Y.Kitaura and K.Tomita for their technical contributions.

REFERENCES

[1]H.P.Singh,et al., GaAs IC Symp., Dig.Tech. Papers, pp.11-14, 1986.
[2]S.Shimizu,et al., ISSCC, Dig.Tech.Papers, pp.52-53, 1984.
[3]T.Terada,et al., IEEE J.Solid-State Circuits, SC-22, NO.5, pp.755-761, 1987.

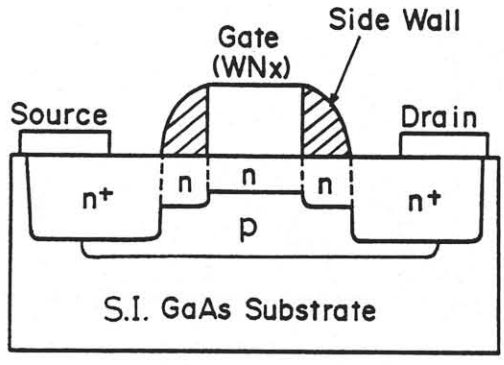


Fig.3 Cross-sectional view of WNx-gate BP-LDD structure

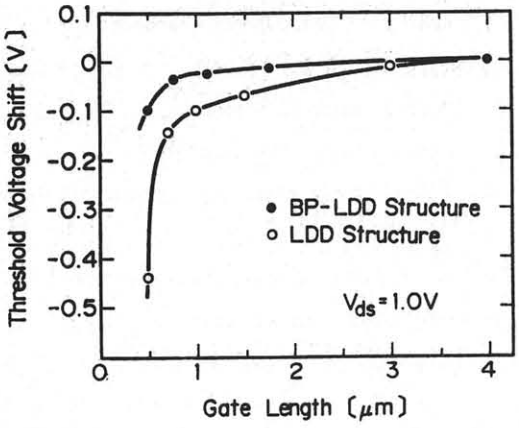


Fig.4(a) Threshold voltage shift dependence on gate length for BP-LDD and LDD structured FETs

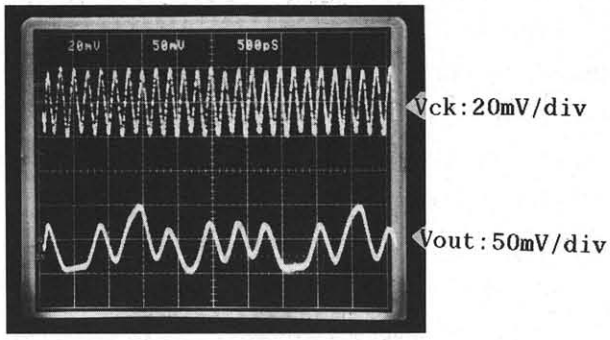


Fig.6 Shift register output (OUT3) waveform at 5 GHz clock frequency for serial input data "0101101001010100"

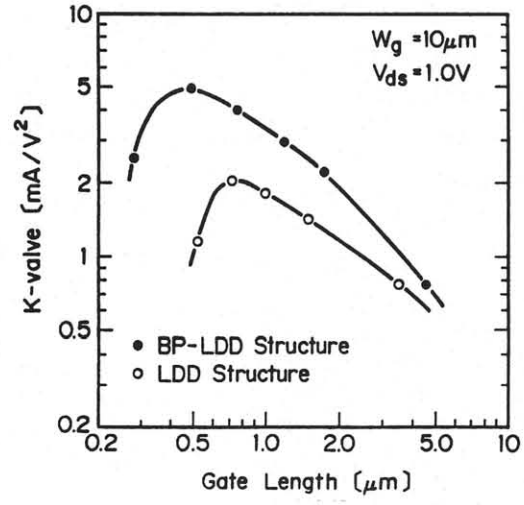


Fig.4(b) K-value dependence on gate length for BP-LDD and LDD structured FETs

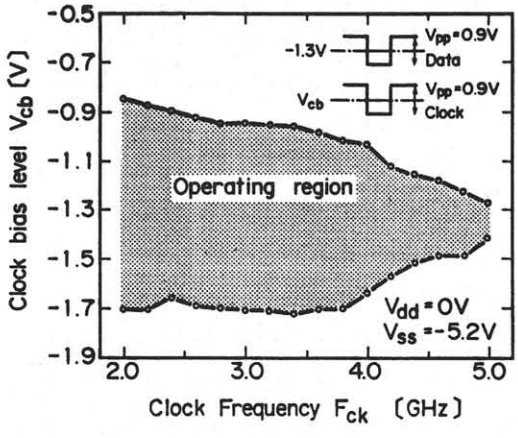


Fig.7 Clock bias margin characteristic of 4-bit shift register

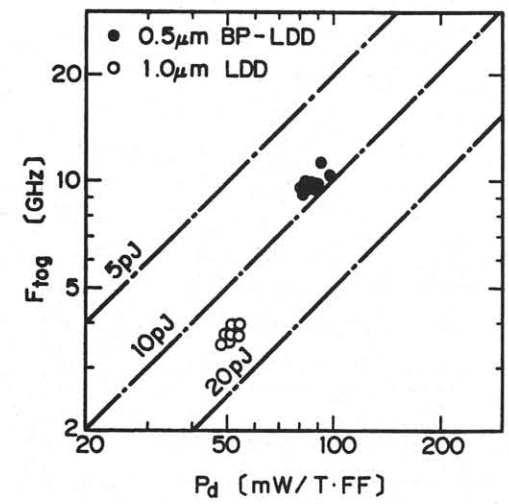


Fig.5 Toggle frequency (Ftog) dependence on power dissipation (Pd) for one T-FF

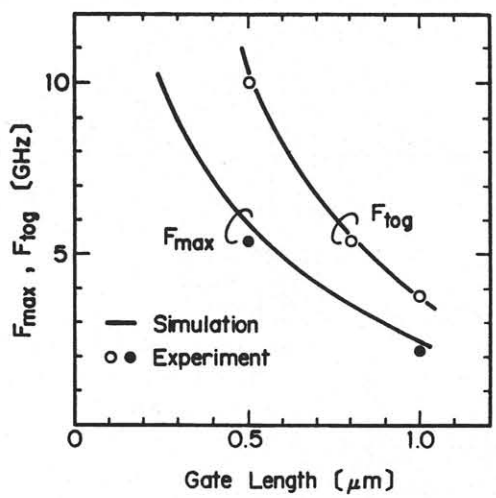


Fig.8 Dependence of maximum operating frequency (Fmax) and toggle frequency (Ftog) on gate length