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4bit A/D and 8bit D/A Converters Implemented with AlGaAs/GaAs HBTs

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This paper describes a 1-chip 4bit A/D and 8bit D/A converter IC, implemented with AlGaAs/GaAs HBT ECL circuits. This IC consisted of about 1200 elements, including resistors, in a $3\times2mm^2$ chip area. The 4bit ADC operated at above 1GHz sampling rate and had a $\pm1/16$LSB static nonlinearity error. The 8bit DAC had a 300psec. rise/fall time and a ±1LSB nonlinearity error.

Introduction

An AlGaAs/GaAs HBT has great potential in regard to application to high speed and high accuracy analog to digital conversion circuits, because of its high intrinsic device speed and excellent threshold voltage uniformity.[1] However, few MSI/LSI level HBT ICs, such as an ADC/DAC, have been fabricated so far, owing to the immaturity of HBT technology.

This paper reports a 1-chip 4bit A/D and 8bit D/A converter IC, implemented with non self aligned AlGaAs/GaAs HBT ECL circuits. This IC operated at an above 1GHz conversion rate. Such high performance was achieved even with relatively large size ($4\times6\,\mu m^2$ emitter) HBTs without self - alignment processing or advanced HBT structures. The measured high accuracy and speed performance show the bright future of high performance HBT A/D and D/A converters.

IC Fabrication

The HBT A/D and D/A converters were fabricated with MBE grown epitaxial layers. The layer structure is shown in Table 1. No advanced HBT structure, such as a graded base or a modulated collector,[2,3] were employed. Fig.1 depicts a cross section of the fabricated non-self-aligned HBT. The n^+ emitter cap layer was isolated by mesa etching. In order to form an external base region for base contact, Mg and P dual ion implantation was carried out. The implanted P ions prevented Mg from diffusing laterally and from causing displacement of the heterojunction and the p-n junction by rapid thermal annealing.[4] The ohmic contacts for the emitter and the collecter were formed with AuGeNi, and for the base with AuZn respectively. Both the inter- and intra-device isolation were made with H and B damage ion implantation. The isolation layer, between the first and the second metal layer interconnection, was a CVD SiO_2 film. A NiCr thin film was used for the load resistors. The minimum emitter size for the fabricated HBTs was $4\times6\mu m^2$. Their cutoff frequency was 20GHz at Ic=2mA.

4bit ADC and 8bit DAC Circuit Design

The fabricated IC consisted of a 4bit ADC,

an 8bit DAC and a data selector. A simplified block diagram of the IC is shown in Fig.2.

The flash ADC had 15 comparators, an encoder for binary code output and 4 latched flip flops. The comparator circuit is shown in Fig.3. Comparator performance is a key to realizing a high speed and high accuracy ADC. The comparator had a gain stage in cascade configuration, usually used in high speed circuits. The reference voltage for 15 comparators was determined by the resistor ladder. The encoder, composed of wired or circuits, made it possible to directly transfer comparator output into a binary code. The circuit diagram for the 8bit DAC is shown in Fig.4. The DAC consisted of an 8bit data latch, matched current sources and current switches. The current switches were composed of a simple differential amplfier pair. For current sources, the current for the upper 4bits was provided by weighted HBTs, scaled to the magnitude of the bit current, in cascade configuration. On the other hand, the lower 4bit current was supplied by same sized HBTs with an R-2R ladder network.

The upper 4bit data to the DAC came from the ADC or the outside of the chip, which could be selected by the data selecter. Using this ADC-DAC loop, the digital output for the ADC could be reconstructed into an analog waveform. Fig.5 shows the fabricated ADC and DAC IC, which consisted of 1200 elements in a $3x2mm^2$ chip area. Its upper portion is the ADC and the lower portion is the DAC with the data selector.

4bit ADC Performance

The fabricated ICs were tested with on wafer probing.

Fig.6 shows the full scale input sine waveform for the ADC and the reconstructed output waveform for the DAC by ADC-DAC loop measurement at 500MHz clock frequency. The output waveform testifies that the ADC quantizes the input signal into 16 4bit levels, appropriately. Its differential linearity error is shown in Fig.7. The error was less than ±8mV, which corresponds to 1/16LSB at a full scale voltage of V=2Vpp. The differential linearity error was probably caused by fluctuating reference resistor values, rather than by the offset voltage among the comparators, because the measured ±2mV offset voltage was less than the ±8mV differential linearity error.

High speed testing was also carried out in the ADC-DAC loop measurement. The input wave to the ADC and the output wave from the DAC at fs=1GHz and fin=100MHz are shown in Fig.8. This shows that sampling the 100MHz input signal functioned accurately and appropriately at 1GHz clock frequency. The comparator performance determines the maximum ADC sampling frequency. Fig.9 depicts a 100kHz beat wave, formed with 500MHz sampling frequency and 500.1MHz input frequency. Although the beat wave had a little harmonic distortion, 4bit accuracy was obtained. This means the input bandwidth for the ADC was over 500MHz. Its total power consumption was 2W.

8bit DAC Performance

Fig.10 shows the DAC transfer function, switching all 256 8bit-levels by inputting the digital ramp data to the DAC. Discontinuities in linearity were observed every time one of the upper 4bits was turned on, which was caused by the difference between the upper 4bit and the lower 4bit current sources in the DAC. These irregularities were clearly depicted in the differential linearity error, as shown in Fig.11. The maximum error was ±1LSB.

High speed testing was made by switching the MSB at 300MHz, because the DAC switching

performance was limited by the largest devices ($4\times6\mu m^2\times8$ emitters) in the circuit. Both (a) the rise form and (b) the fall form for the output signals are shown in Fig.12. The measured rise and fall time were approximately 300psec, which means the fabricated DAC is capable of operating up to 2GHz sampling frequency. The ringing phenomenon was observed in each of the output forms. These were probably caused by the inductance resonance in the probe card at above 1 GHz. The total power consumption, for the DAC with the data selector, was 1.3W.

Table.1 Epitaxial layer structure for HBTs

		Thickness (nm)	Doping (cm^{-3})
Cap	n-GaAs	100	5E18
Grading	n-AlGaAs	30	5E17
Emitter	n-$Al_{0.3}Ga_{0.7}As$	150	5E17
Grading	n-AlGaAs	50	5E17
Base	p-GaAs	100	5E18
Collecter	n-GaAs	550	3E16
Sub-collecter	n-GaAs	550	3E18

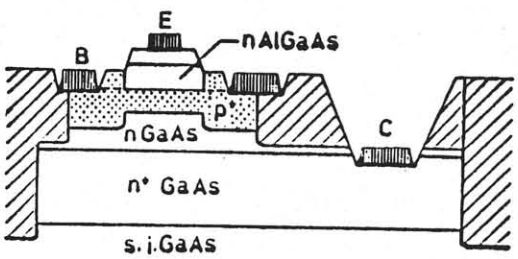


Fig.1 Schematic cross section of HBT

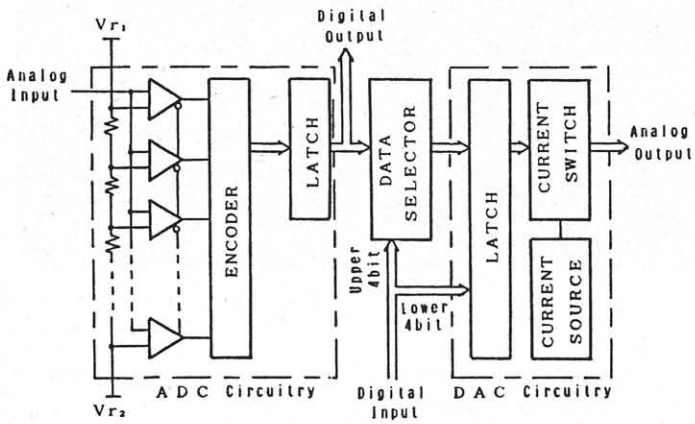


Fig.2 An IC blockdiagram

Conclusion

High performance 4bit A/D and 8bit D/A conversion circuits have been successfully realized with AlGaAs/GaAs HBTs. The ADC and the DAC have over 1GHz and over 2GHz sampling capabilities, respectively. Such high performance was achieved with relatively large size non-self-aligned HBTs, without any advanced structure. The simplified HBT technology is very attractive for 1-2GHz data conversion. A combination of the recently developed high yield self alignment HBT processing and the newly proposed modulated collector structure will make dramatic improvement in the data conversion rate and has a potential to make a 5-10GHz ADC/DAC a reality, rather than a concept.

Reference

1)K.C.Wang; GaAs IC Symp.1987,pp83-86

2)T.Ishibashi; 45th.Dev.Res.Conf.1987 IV-6

3)K.Morizuka; 46th.Dev.Res.Conf.1988 IVA-2

4)K.Morizuka; 18th Conf.Solid State Devices and Materials,pp359-362

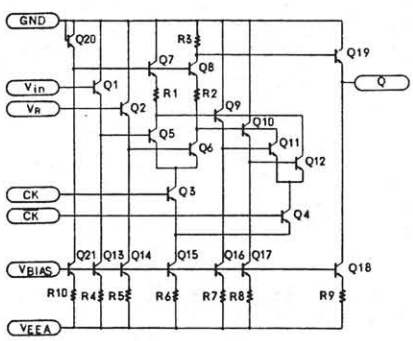


Fig.3 Circuit diagram of comparator

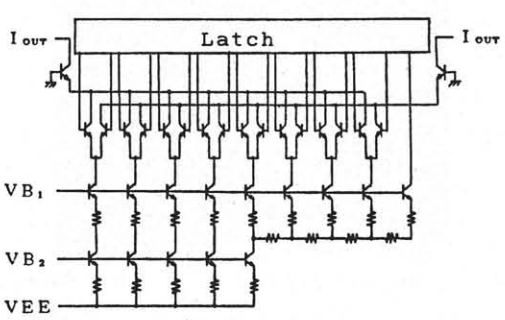


Fig.4 Circuit diagram of 8bit DAC

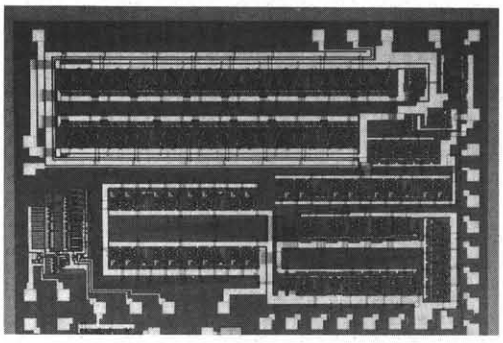


Fig.5 Fabricated HBT IC

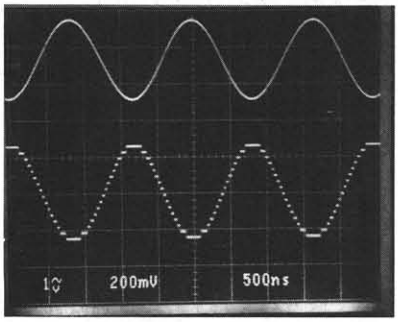


Fig.6 Input sine wave to ADC (top)
Reconstructed sine wave from DAC (bottom)
(fs=500MHz)

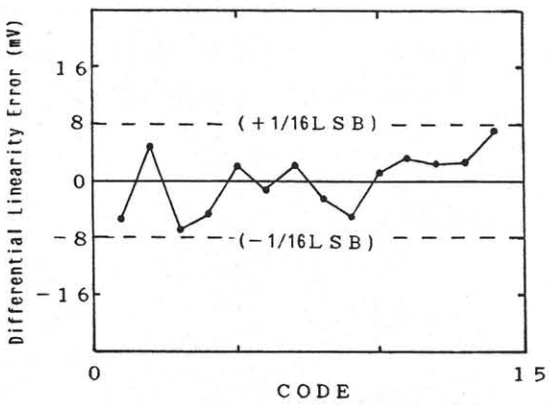


Fig.7 4bit ADC differential linearity error

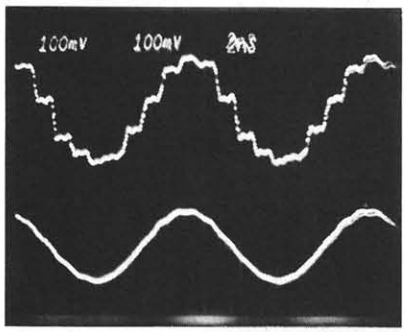


Fig.8 Reconstructed sine wave from DAC (top)
Input sine wave to ADC (bottom)
(fin=100MHz, fs=1GHz)

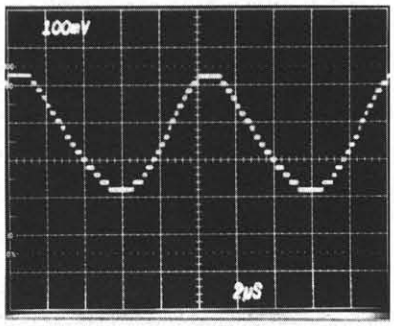


Fig.9 DAC output beat wave
(fin=500.1MHz, fs=500MHz)

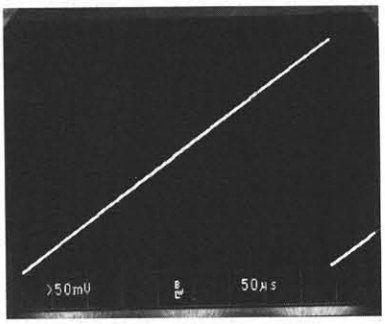


Fig.10 8bit DAC transfer function

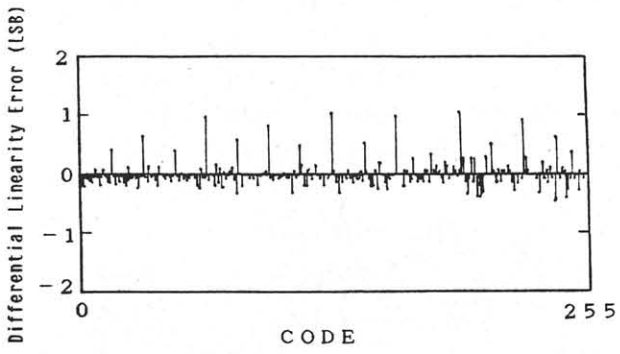
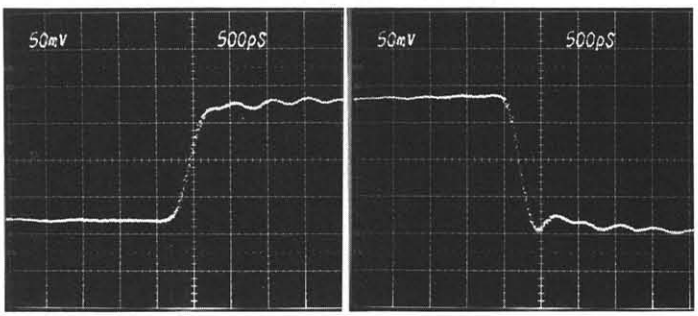


Fig.11 8bit DAC differential linearity error



(a) Rise waveform (b) Fall waveform

Fig.12 DAC output wave, as switching MSB at 300MHz