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Analysis of Two-Dimensional Effects on Switching Delay Time for Emitter Coupled Logic Circuits

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Emitter coupled logic (ECL) gate delay for submicrometer transistors was investigated with a focus on the current and hole distribution, using a newly developed device simulator, which can set a constant current source. From the simulation results, microscopic two-dimensional behavior in transistors was directly connected to the ECL circuit performance for the first time.

1. INTRODUCTION

Commonly used circuit simulators and analytical methods which implement the Gummel-Poon model, Ebers-Moll model or those variants are not sufficiently exact for obtaining the emitter coupled logic (ECL) gate delay.[1-4] Therefore, it has been very difficult to incorporate circuit performance information into the microscopic transistor design.[5]

Recently, a two-dimensional numerical method was introduced to ECL and deeper insight into the device operation was obtained.[6] However, a constant current source, which is ordinarily used for an ECL power supply, was replaced by a resistor, owing to the restriction on the electrode boundary conditions.

In this paper, the authors demonstrate a two-dimensional transient analysis for ECL circuits, using a newly developed device simulator, which can set a constant current source.

2. SIMULATED GATE STRUCTURE AND CONDITIONS

Figure 1 shows the cross-sectional geometry for half of the transistors. The emitter area was 0.4 x 6 μm^2. NOR and OR transistors were placed against each other, separated electromagnetically, except for the emitter electrode, by an oxide with reflective boundary conditions on line a-a'.

The collector-substrate capacitance C_{TS} was placed as a 10fF external parameter. This setting up is valid, because the n^+ buried collector layer resistivity was so small that current distribution was uniform and C_{TS} was independent from the current level. The collector load resistance R_C, the constant current source I_E, and the logic swing V_1 were 600 ohms, 1 mA, and 0.6 V, respectively.

The minimum grid spacing was 5 nm at the emitter-base peripheral region, where the two-dimensional effect plays an important role in regard to the transient property. There were 4116 grid points for the whole region.

3. SIMULATION RESULTS AND DISCUSSIONS

Figure 2 shows the input, output and emitter voltage transient waveforms in the case of OR transistor turn-on. In this case, simulation was performed without the collector-substrate capacitance C_{TS}, in order to clearly observe the two-dimensional effect on the gate delay. The output voltage V_{C2} decreased, as soon as the input voltage V_{B1} ramp-down started (the base-collector voltage V_{BC1} increased), and increased to its steady state. The V_{C1} change was retarded during V_{B1} ramp-down. Recently, the authors have reported that the turn-off transient for a bipolar transistor is faster than the turn-on transient, due to the difference between the excess carrier discharge and charge mechanisms.[7] Accordingly, it can be said that the ECL gate delay is controlled by the turn-on transistor. In this work, therefore the turn-on transistor behavior was mainly observed.

The output transient curve V_{C2} can be divided into four periods. In the first period till 14 ps lapsed time, there is little change. During this period, the base current vector concentrates in the emitter side wall region and the junction capacitance for this region is charged, as shown in the top profile in Fig.3. After input voltage ramp-down is stopped, holes begin to diffuse into the emitter sidewall and V_{C2} decreases linearly in period II. Passing the half way point in the logic swing voltage, V_{C2} gradually rolls off in region III, where holes also flow toward the base-collector junction.

Figure 4 shows the hole distribution profiles for 6, 12 and 30 ps lapsed times. Comparing these figures with each other, it is observed that the emitter sidewall is charged at 12 ps lapsed time and Kirk's base widening occurs at 30 ps lapsed time.

As mentioned previously, in period II, V_{C2} decreases linearly, which indicates that the CR time constant, due to the base response, gradually decreases. This can be attributed to Kirk's base widening. Namely,

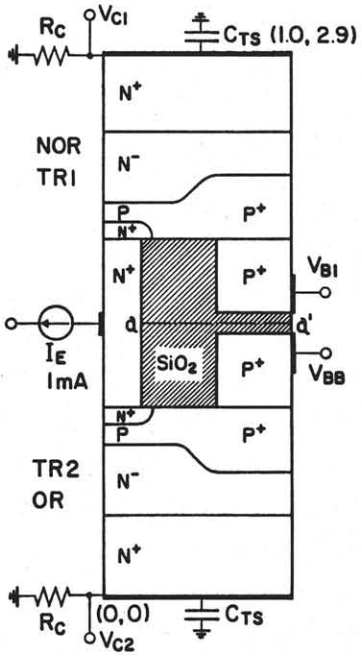

Fig.1 Cross-sectional geometry for half of the simulated transistors, with external circuit parameters.

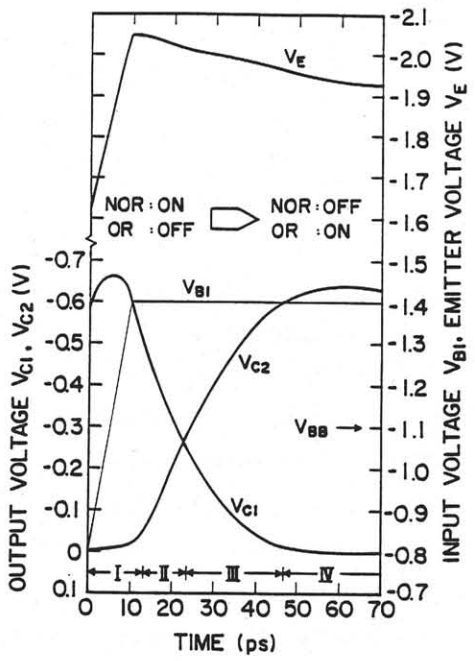

Fig.2 Input(V_{B1}), output(V_{C1} and V_{C2}) and emitter(V_E) voltage transient waveforms in the case of OR transistor turn-on.

the decrease in the base resistance $r_{bb'}$ is larger than the increase in the junction capacitance C_{TE} and the diffusion capacitance C_d.

In period III, C_d continues to increase and $r_{bb'}$ saturates. Thus the CR time constant gradually increases.

In period IV, V_{C2} exceeds the final value. This phenomenon is typical for an ECL with a constant current source. The emitter-base voltage V_{BE2} at 10 ps lapsed time, when the input voltage ramp-down stops, is larger than the final value (see the I_E curve in Fig.2), as is the concentration of holes stored around the emitter sidewall. As a result, holes, mainly stored at the emitter sidewall, flow out to the base contact, until the hole concentration reaches a final steady state value, as shown in Fig.5.

The output voltage transient form V_{C1} for NOR transistor turn-on is shown with V_{C2} for OR transistor turn-on in Fig.6. For NOR transistor turn-on case, V_{C1} changes its sign, just after input voltage ramp-down starts, to 12 ps lapsed time. This is due to quasi-saturation. This state continues until 12 ps have lapsed. However, there is little difference between the V_{C1} and V_{C2}

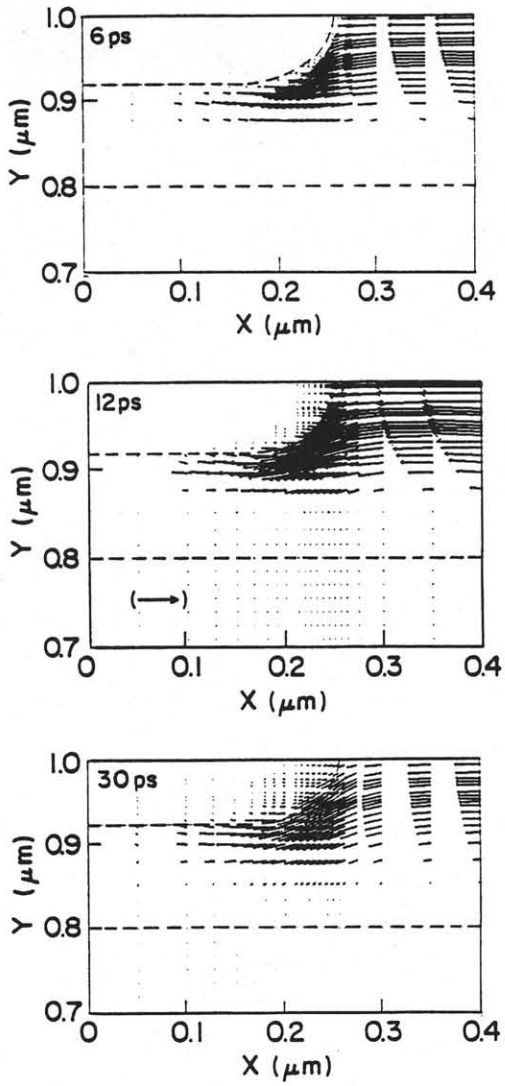

Fig.3 Hole current vector distributions around the OR-transistor emitter-base junction at 6, 12, and 30 ps lapsed times. The arrow (→) indicates the unit hole current density of 3 x 10^3 A/cm^2.

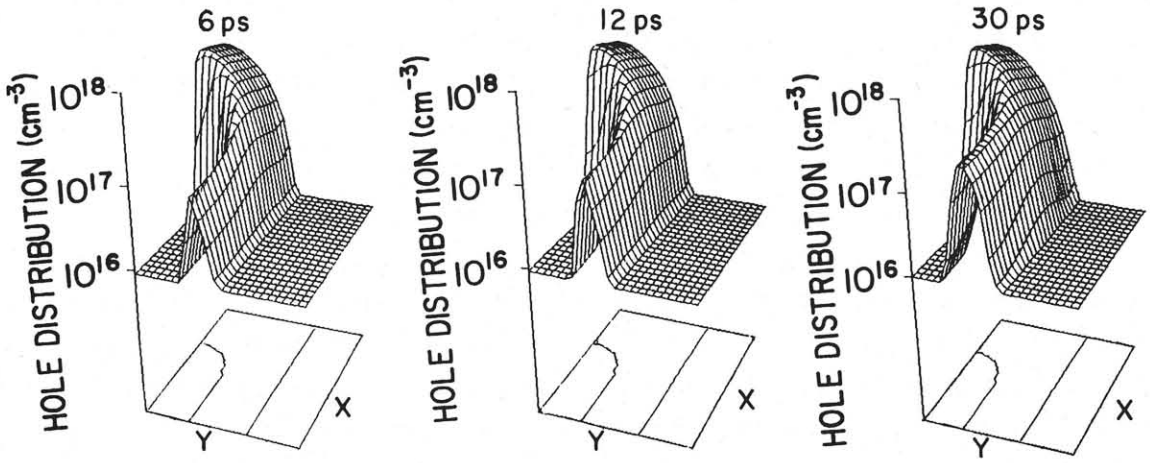

Fig.4 Hole distribution stereographs around the OR-transistor emitter-base junction at 6, 12, and 30 ps lapsed times. Hole densities under 1 x 10^{16} cm^{-3} are cut off.

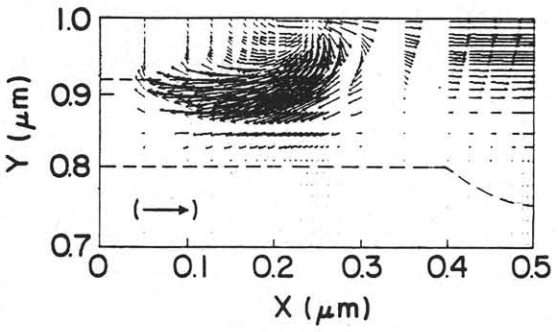

Fig.5 Hole current vector distributions around the OR-transistor emitter-base junction at 60 ps lapse time. The arrow (→) indicates the unit hole current density of 3 x 10^3 A/cm^2.

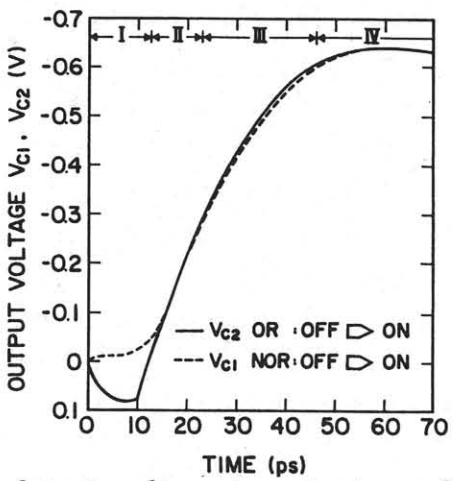

Fig.6 Output voltage transient waveforms V_{C1} and V_{C2} for NOR transistor and OR transistor turn-on, respectively.

curves after period I. This indicates that the quasi-saturation state has no influence on the gate delay and that the base response dominates the gate delay.

Finally, ECL gate delay was simulated with C_{TS}. The gate delay due to C_{TS}, determined for the half way point in the logic swing, was 5.7 ps, which was almost equal to the $C_{TS}R_C$ product of 6 ps. Furthermore, in the NOR transistor turn-on case with C_{TS}, quasi-saturation was also independent from the delay time.

5. CONCLUSIONS

This paper has attempted to show the two-dimensional behavior in switching transitions for an ECL, using a simulator extended from the device to the gate level. From the simulation results and discussion, the following conclusions were reached.

(1) The two-dimensional Kirk's base widening at the emitter corner, which causes a decrease in $r_{bb'}$ and an increase in diffusion capacitance as time elapses, is the major cause for gate delay.

(2) Collector current overshoot was observed for the turn-on transistor output. This is due to the discharge of excess carriers, stored during the input voltage ramp-down period.

(3) Quasi-saturation for the NOR transistor has no influence on the gate delay, because this state is independent from the base response.

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