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Characteristics of Bipolar Transistors with Various Depth n^+ Buried Layers Formed by High Energy Ion Implantation

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Bipolar transistors having various depth n^+ buried layers formed by high energy ion implantation are investigated in order to obtain various performance bipolar transistors in the same chip. BV_{CEO} values are controlled and decreased with increasing oxide thickness by high-energy ion implantation in Si dioxide film of varying thicknesses. The maximum obtained BV_{CEO} value is 7.8V. Base-collector leakage currents are very small when secondary defects are buried in the n^+ buried layer. This method should be very effective for designing both BiCMOS and multi-function LSIs.

1. Introduction

BiCMOS LSIs are very promising LSIs because they have both high speed and low power dispersion characteristics[1),7)]. High performance npn bipolar transistors used for BiCMOS LSIs require n^+ buried layers. Since n^+ buried layers are necessary for many processes, like Si epitaxial growth, layer formation production cost is high. Therefore the cost of n^+ buried layers has limited BiCMOS LSI technology application. Another drawback is that the performance of bipolar transistors used for BiCMOS LSIs is uniform in the same chip because the depth of n^+ buried layers is solely decided by Si epitaxial layer thickness. Under uniform conditions, it is difficult to achieve high speed and multi-functionable BiCMOS LSIs.

This paper proposes the formation of varying depth n^+ buried layers in the same chip using a high energy ion implantation (HEI[2]) technique[2),3),4)] in order to achieve lower cost-, high speed-, multi-function-BiCMOS LSIs. The varying depth n^+ buried layers formed by high-energy ion implantation in SiO_2 film of varying thickness, and the varying performance bipolar transistors obtained, are reported.

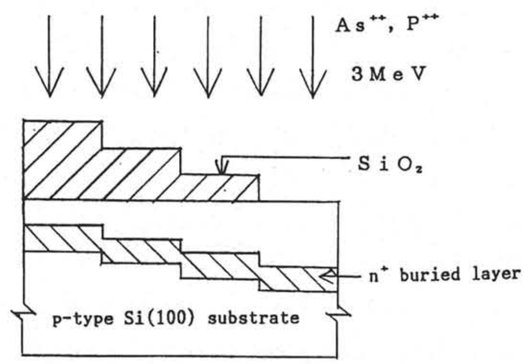

Fig. 1 Procedure of making various depth n^+ buried layers

2. Experiments

The formation method of various n^+ buried layers is shown in Fig. 1. Si dioxide film of various thickness (0, 0.2, 0.4, 0.6μm) formed on the p-type Si substrate. As^{++} or P^{++} ions are implanted into the Si substrate through the varying thickness SiO_2 films. Using this process, various depth n^+ buried layers can be obtained at the same implantation condition and in the same wafer, because implanted ions lose energy while passing through varying thickness SiO_2 film. Acceleration energy is 3MeV. When the implanted ion is phosphorous, ion implanted depth are about 2.5, 2.3, 2.1, 1.9μm. The P^{++} ions' dose was $7\times10^{14}/cm^2$. With this P^{++} dose, the n^+ buried layer resistance is thought to be equal to that of conventional Si epitaxial substrates. When n^+ buried layers are formed by HEI^2 for bipolar transistors, leakage current problem exists in base-collector junctions. Therefore, annealing in N_2 atmosphere was performed before the oxidation process[5]. Annealing temperature was 1000℃ and annealing time was 30min. Next, the poly-Si emitter bipolar transistor was fabricated by the conventional bipolar transistor's process.

3. Results and Discussion

Simulated arsenic and phosphorous profiles before and after annealing (1000℃, 180min.) are depicted in Fig. 2. As shown in this figure, the phosphorous profile is deeper than that of arsenic. This result means that phosphorous ions are superior to arsenic ions in achieving large BV_{CEO} value. Arsenic ions have a small diffusion constant, small R_P value and a large ΔR_P value. On the other hand, phosphorous ions have a large diffusion constant value, large R_P value, a small ΔR_P value. In HEI^2, since ion dispersion is very large, the impurity diffusion drive-force is very small. Therefore the R_P factor is most important in obtaining large BV_{CEO} values. Simulated bipolar transistor impurity profiles are indicated in Fig. 3. The P^{++} ions dose is $7\times10^{14}/cm^2$. R_P and ΔR_P values of HEI^2 were used as the experimental values[6], and R_P values were supposed to decrease by the same value as the oxide thickness. Fig. 4(a) indicates the relationship between collector current(I_C) and the applied voltage between collector and emitter(V_{CE}) for P^{++} ions, Fig. 4(b) is for As^{++} ions. In the case of As^{++} ions, the dose is $1.7\times10^{15}/cm^2$. Both ions are directly implanted in the Si substrate not passing through the SiO_2 film.

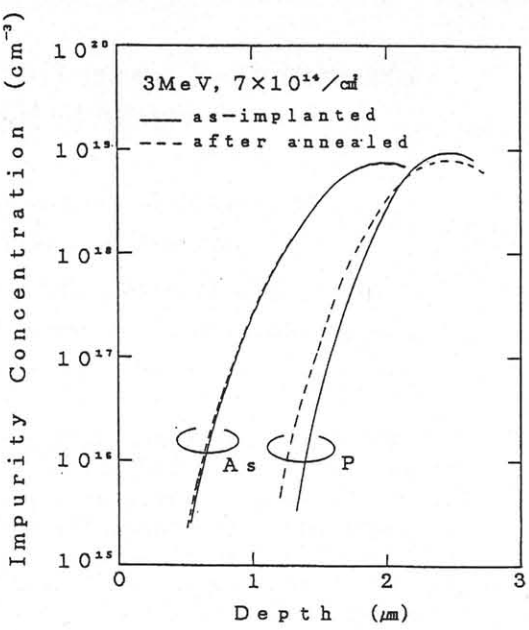

Fig. 2 Simulated phosphorous and arsenic profiles before and after annealing (1000℃, 30min.)

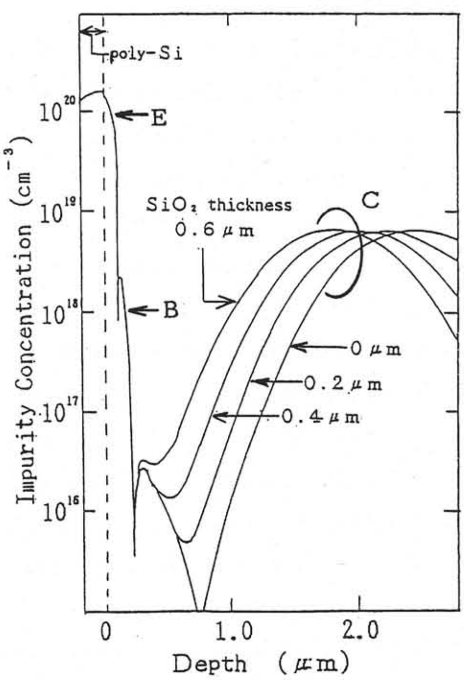

Fig. 3 Simulated impurity profiles in case of various oxide thicness for P^{++} ions(3MeV, $7\times10^{14}/cm^2$)

Figs. 4(a) and (b) reveal that the breakdown voltage between the emitter and collector in the case of P^{++} ions, is larger than the value in the case of As^{++} ions. This result is coincident with the result in

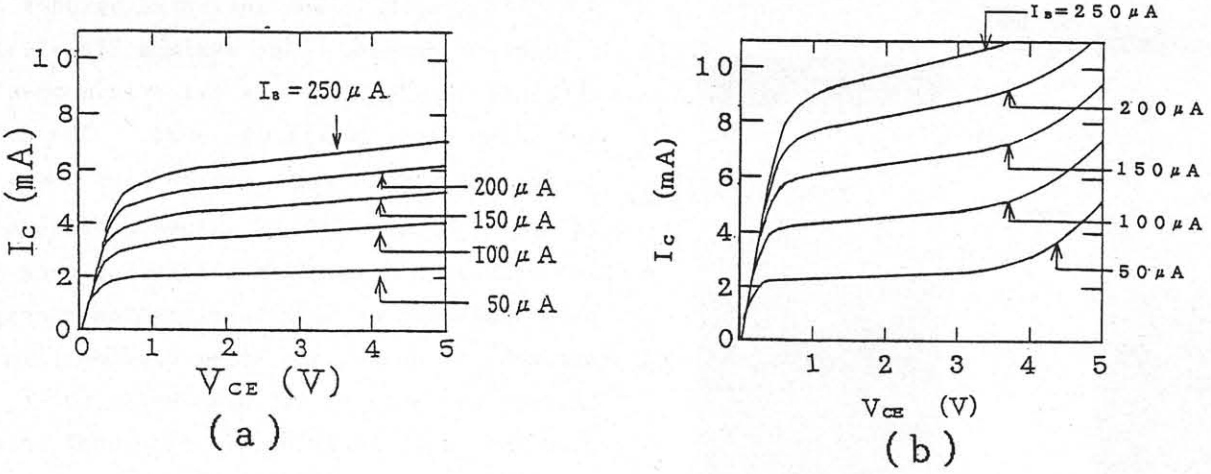

Fig. 4 Collector current versus collector-emitter voltage for (a) As^{++} ions and (b) P^{++} ions (emitter size : $1\times3\mu m^2$)

Fig. 2. The collector resistance(R_{CS}) values examined from V_{CE}-I_C saturation region characteristics are 140Ω in the case of P^{++} ions and 110Ω in case of As^{++} ions. These values are smaller than the R_{CS} value (180Ω) for bipolar transistors formed in conventional Si epitaxial substrates, the same process used with HEI^2. The relationship between BV_{CEO} values and oxide thickness is shown in Fig. 5. This result reveals that the BV_{CEO} values are easily controlled by Si dioxide film thickness. This result also shows that BV_{CEO} values decrease linearly as oxide thickness increases. The BV_{CEO} maximum value was 7.8V for P^{++} ions and 4.4V for As^{++} ions. The base-collector leakage currents histogram for HEI^2 and the leakage currents histogram for conventional Si epitaxial substrate used as a reference, are shown in Fig. 6.

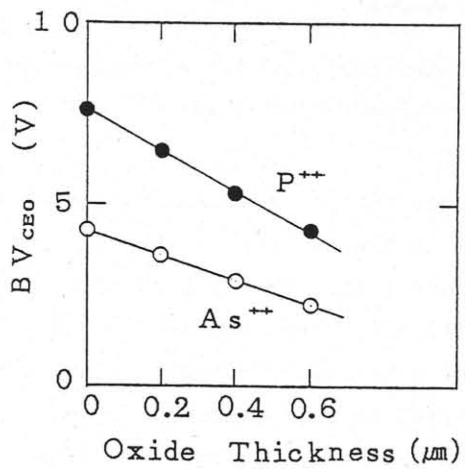

Fig. 5 Dependence of BV_{CEO} values on oxide thickness for As^{++} ions and P^{++} ions

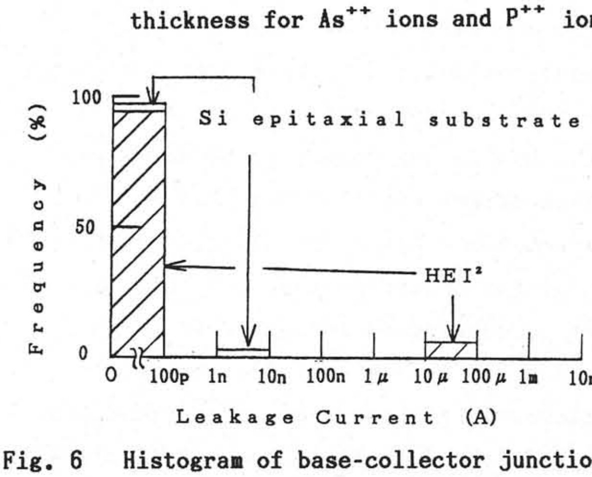

Fig. 6 Histogram of base-collector junctions' leakage currents at V_{BC} of 5V for HEI^2 and Si epitaxial substrate

Measurement conditions of leakage currents are as follows. The base-collector junction area size is $60\mu m\times150\mu m$, and the reverse bias value is 5V. This figure reveals that leakage current values for HEI^2 are less than 100pA in over 90% of measured devices. This rate is nearly the same as the conventional Si epitaxial substrate case. However, large leakage currents (30μA) exists in the HEI^2 case. This large leakage current value exceeds that of the epitaxial substrate (4.3nA), and the frequency is also a little larger. Cross-sectional TEM(XTEM) micrographs of the same sample as for the

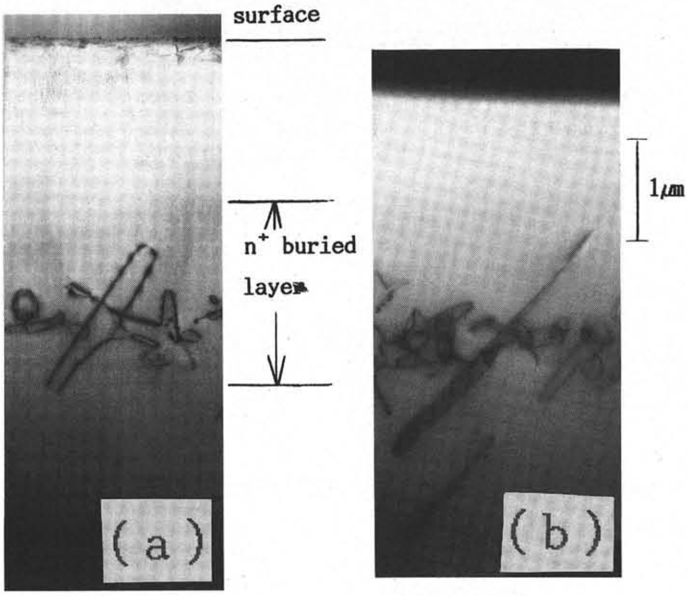

Fig. 7 Cross-sectional TEM micrographs of secondary defects for P^{++} ions

HEI² leakage current measurement are shown in Fig. 7. In Fig. 7, the n^+ buried layer defined by the region in which phosphorous concentration is more than $1\times10^{18}/cm^3$ is also indicated. Secondary defects exist inside the n^+ buried layer for the most part (region(a)), as shown in Fig. 7. This result is thought to be the reason for the low leakage currents (below 100pA). That is, the base-collector depletion region does not reach the secondary defects buried in the n^+ buried layer. On the other hand, a large rod-like defect was also observed (region(b)). This defect almost reaches the front of the n^+ buried layer. This type of defect is considered to result in large leakage currents, as mentiond above. Therefore, it is necessary to eliminate these large rod-like defects to completely eliminate large leakage currents. Finally, remaining secondary defects are proved to be harmless, if they are deeply imbedded in the n^+ buried layer.

4. Conclusion

In conclusion, high-grade n^+ buried layers were confirmed to be made by $7\times10^{14}/cm^2$ of P^{++} ions implanted by 3MeV acceleration energy. The maximum BV_{CEO} value obtained was 7.8V. This value is a practical value never before achieved. The collector resistance value can be less than 140Ω. Moreover, BV_{CEO} values decreased linearly with oxide film thickness, when ions were implanted by high acceleration energy through various thickness Si dioxide film. Leakage currents of the base-collector junction were significantly decreased when thermal annealing (1000℃, 30min.) was performed in N_2 atmosphere. The method of HEI² described in this paper should be a very effective process for designing both BiCMOS- and multi-function LSIs.

Acknowledgments

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